## **EXHIBIT 19**

## EXHIBIT 19

## **UNITED STATES PATENT NO. 7,231,474**

MediaTek hereby identifies evidence demonstrating the infringement of following NXP products: NXP Sensors specifically including but not limited to FXOS8700CQ, FXLS8962AF, FXPS7115D4 (the "Accused '474 Sensors"); NXP wireless microcontrollers specifically including but not limited to K32W061 and K32W041 (the "Accused '474 Wireless Microcontrollers"); and NXP i.MX Applications Processors specifically including but not limited to i.MX6 Dual and i.MX6 Quad (the "Accused '474 i.MX Processors") (collectively, the "Accused '474 products"). The chart below is based on evidence of representative products of the Accused '474 Products.

'474 Patent Claim	Representative NXP Product(s)
[1a.] A serial communication system comprising:	To the extent the preamble is limiting, the Accused '474 Sensors include a "serial communication system" as recited in the '474 patent. Exemplary systems and serial interfaces are identified in the block diagrams and rectangles below.
	See, e.g.,
	FX058700CQ

'474 Patent Claim	Representative NXP Product(s)
	https://www.avnet.com/shop/us/products/nxp/fxos8700cqr1-
	3074457345626313537? from Page= autoSuggest& langId = -1& autoSuggestSearchTerm = FXOSE auto
	Image: Second
	SLN-RPK-NODE (development board of FXOS8700CQ) (Arrow)
	25 25 25 25 25 25 25 25 25 25





















'474 Patent Claim	Representative NXP Product(s)		
	10.1.2 I <sup>2</sup> C read/write operations		
	The master transmits a start condition (ST) to FXLS8962AF, followed by the slave address, with the R/W bit set to '0' for a write, and the FXLS8962AF sends an acknowledgement. Then the master transmits the address of the register to read and the FXLS8962AF sends an acknowledgement. The master transmits a repeated start condition (SR), followed by the slave address with the R/W bit set to '1' for a read from the previously selected register. The FXLS8962AF then acknowledges and transmits the data from the requested register. The master does not acknowledge (NAK) the transmitted data and then transmits a stop condition to end the data transfer.		
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18.		
	11 SPI interface The SPI interface is a classical Master/Slave serial port. FXLS8962AF is always considered to be the slave device and thus never initiates communication with the host		
	The SPI interface of FXLS8962AF is compatible with interface mode 00, corresponding to CPOL = 0 and CPHA = 0		
	For CPOL = 0, the idle value of the clock is zero, and the active value of the clock is 1. For CPHA = 0, data is captured on the clock's rising edge (low to high transition) and data is propagated on the clock's falling edge (high to low transition).		
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 20.		
	10.1.1 General I <sup>2</sup> C operation There are two signals associated with the I <sup>2</sup> C-bus: the Serial Clock Line (SCL) and the Serial Data line (SDA). SDA is a bidirectional signal used for sending and receiving the data to/from the interface. External pull-up resistors connected to V <sub>DD</sub> are required for SDA and SCL. When the I <sup>2</sup> C-bus is free, SCL and SDA are high.		

'474 Patent Claim	Representative NXP Product(s)		
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18.		
	11.1 General SPI operation         The SPI_CS_B pin is driven low at the start of a transaction, held low for the duration of the transfer, and then driven high again after the transaction is completed. During a transaction, the master toggles the clock (SCLK). The SCLK polarity is defined as having an idle value that is low, and an active phase that is high (CPOL = 0). Serial input and output data is captured on the clock's rising edge and propagated on the falling edge         EXI S8962AE       3-Axis Low-g Accelerometer. Product data sheet (Rev. 5.3 — 10 December 2019) at 20		
	<ul> <li>11.4 SPI read operations with 3-wire mode</li> <li>FXLS8962AF can be configured to operate in 3-wire software enabled SPI mode. In this mode, the SPI_MISO pin is left unconnected and the SPI_MOSI pin becomes a bidirectional input/output pin (SPI_DATA). Read operations in 3-wire mode are the same as write operations in 3- and 4-wire modes, except that at the end of the address cycle (falling edge of clock pulse 16), the SPI_DATA pin automatically switches from an input to an output and with bit D7 as the current output state.</li> <li>FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 22.</li> </ul>		



'474 Patent Claim	Representative NXP Product(s)		
	10.1.2 I <sup>2</sup> C read/write operations Single-byte read The master (or MCU) transmits a start condition (ST) to the FXOS8700CQ, followed by the slave address, with the R/W bit set to "0" for a write, and the FXOS8700CQ sends an acknowledgement. Then the master (or MCU) transmits the address of the register to read and the FXOS8700CQ sends an acknowledgement. The master (or MCU) transmits		
	a repeated start condition (SR), followed by the slave address with the R/W bit set to "1" for a read from the previously selected register. The FXOS8700CQ then acknowledges and transmits the data from the requested register. The master does not acknowledge (NAK) the transmitted data, but transmits a stop condition to end the data transfer. FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer, Data sheet: Technical data (Rev. 8 — 25 April 2017) at 15.		
	10.1.1 General I <sup>2</sup> C operation There are two signals associated with the I <sup>2</sup> C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. External pullup resistors connected to VDDIO are required for SDA and SCL. When the bus is free both the lines are high. The I <sup>2</sup> C interface is compliant with fast mode (400 kHz), and normal mode (100 kHz) I <sup>2</sup> C standards. Operation at frequencies higher than 400 kHz is possible, but depends on several factors including the pullup resistor values, and total bus capacitance (trace + device capacitance). See <u>Table 11</u> for more information.		
	FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer, Data sheet: Technical data (Rev. 8 — 25 April 2017) at 14.		

'474 Patent Claim	Representative NXP Product(s)			
	10.2.1 General SPI operation			
	NOTE			
	FXOS8700CQ only supports a point-to-point SPI protocol, with only one master (MCU) and one slave device (FXOS8700CQ) present on the bus. FXOS8700CQ does not tri-state the MISO pin when the CS_B pin is deasserted (logic high), which can lead to a bus conflict if multiple slave devices are present on the bus.			
	Do not connect more than one master and one slave device on the SPI bus.			
	The CS_B pin is driven low at the start of a SPI transaction, held low for the duration of the transaction, and driven high after the transaction is complete. During a transaction the master toggles the SPI clock (SCLK) and transmits data on the MOSI pin.			
	FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer, Data sheet: Technical data (Rev. 8 — 25 April 2017) at 17.			



'474 Patent Claim	Representative NXP Product(s)			
	7.4.1 I <sup>2</sup> C bit transmissions The state of SDA when SCL is high determines the bit value being transmitted. SDA must be stable when SCL is high and change when SCL is low as shown in <u>Figure 14</u> . After the START signal has been transmitted by the master, the bus is considered busy. Timing for the start condition is specified in <u>Table 105</u> .			
	FXPS7115D4, Digital absolute pressure sensor, 40 kPa to 115 kPa, Product data sheet (Rev. 4 — 17 July 2020) at 13.			
	<ul> <li>7.5 Standard 32-bit SPI protocol         The device includes a standard SPI protocol requiring 32-bit data packets. The device is a slave device and requires that the base clock value be low (CPOL = 0) with data captured on the rising edge of the clock and data propagated on the falling edge of the clock (CPHA = 0). The most significant bit is transferred first (MSB first). SPI transfers are completed through a sequence of two phases. During the first phase, the command is transmitted from the SPI master to the device. During the second phase, response data is transmitted from the slave device. MOSI and SCLK transitions are ignored when SS_B is not asserted.     </li> <li>FXPS7115D4, Digital absolute pressure sensor, 40 kPa to 115 kPa, Product data sheet (Rev. 4 — 17 July 2020) at 17.</li> </ul>			
[1c.] a processor having a slave serial interface coupled to the master serial interface through a clock signal line and a data signal line	The Accused '474 Sensors each includes a processor having a slave serial interface coupled to the master serial interface through a clock signal line and a data signal line. For example, the Accused '474 Sensors each includes a processor having a slave serial interface ( <i>e.g.</i> , SPI/I2C) coupled to the master serial interface identified above through a clock signal line ( <i>e.g.</i> , the serial clock line (SCL) and/or the SPI clock (SCLK)) and a data signal line ( <i>e.g.</i> , the serial data line (SDA) and/or the SPI master serial data out slave serial data in (MOSI)).			



'474 Patent Claim	Representative NXP Product(s)	
	10.1.2 I <sup>2</sup> C read/write operations 10.1.2.1 Single byte read	
	The master transmits a start condition (ST) to FXLS8962AF, followed by the slave address, with the R/W bit set to '0' for a write, and the FXLS8962AF sends an acknowledgement. Then the master transmits the address of the register to read and the FXLS8962AF sends an acknowledgement. The master transmits a repeated start condition (SR), followed by the slave address with the R/W bit set to '1' for a read from the previously selected register. The FXLS8962AF then acknowledges and transmits the data from the requested register. The master does not acknowledge (NAK) the transmitted data and then transmits a stop condition to end the data transfer.	
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019	)) at 18.
	11 SPI interface	
	The SPI interface is a classical Master/Slave serial port. FXLS8962AF is always considered to be the slave device and thus never initiates communication with the host processor.	
	The SPI interface of FXLS8962AF is compatible with interface mode 00, corresponding to CPOL = 0 and CPHA = 0.	
	For CPOL = 0, the idle value of the clock is zero, and the active value of the clock is 1. For CPHA = 0, data is captured on the clock's rising edge (low to high transition) and data is propagated on the clock's falling edge (high to low transition).	
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019	9) at 20.
	10.1.1 General I <sup>2</sup> C operation There are two signals associated with the I <sup>2</sup> C-bus: the Serial Clock Line (SCL) and the Serial Data line (SDA). SDA is a bidirectional signal used for sending and receiving the data to/from the interface. External pull-up resistors connected to V <sub>DD</sub> are required for SDA and SCL. When the I <sup>2</sup> C-bus is free, SCL and SDA are high.	

'474 Patent Claim	Representative NXP Product(s)		
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18.		
	11.1 General SPI operation         The SPI_CS_B pin is driven low at the start of a transaction, held low for the duration of the transfer, and then driven high again after the transaction is completed. During a transaction, the master toggles the clock (SCLK). The SCLK polarity is defined as having an idle value that is low, and an active phase that is high (CPOL = 0). Serial input and output data is captured on the clock's rising edge and propagated on the falling edge         EXI S8962AE       3-Axis Low-g Accelerometer. Product data sheet (Rev. 5.3 — 10 December 2019) at 20		
	<ul> <li>11.4 SPI read operations with 3-wire mode</li> <li>FXLS8962AF can be configured to operate in 3-wire software enabled SPI mode. In this mode, the SPI_MISO pin is left unconnected and the SPI_MOSI pin becomes a bidirectional input/output pin (SPI_DATA). Read operations in 3-wire mode are the same as write operations in 3- and 4-wire modes, except that at the end of the address cycle (falling edge of clock pulse 16), the SPI_DATA pin automatically switches from an input to an output and with bit D7 as the current output state.</li> <li>FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 22.</li> </ul>		

'474 Patent Claim	Representative NXP Product(s)		
	SDA / SPI_MOSI / SPI_DATA	4	<ul> <li>Mode dependent Multifunction serial interface pin.<sup>[2]</sup></li> <li>INTF_SEL = V<sub>DD</sub>:</li> <li>SPI_MOSI: In 4-wire SPI mode this pin functions as the serial data input (Master Out Slave In).</li> <li>SPI_DATA<sup>[3]</sup>: In 3-wire SPI mode this pin functions as the bidirectional serial data input/output.</li> <li>INTF_SEL = GND:</li> <li>SDA: This pin functions as the I<sup>2</sup>C Serial Data input/output.</li> </ul>
	SCL/SCLK FXLS8962AF, 3-Axis Lo	5 w-g Ac	Mode dependent Multifunction serial interface pin. <sup>[2]</sup> INTF_SEL = V <sub>DD</sub> : • SPI serial clock input (3- and 4-wire modes) INTF_SEL = GND: • I <sup>2</sup> C serial clock input ccelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 4.



'474 Patent Claim	Representative NXP Product(s)		
	10.1.2 I <sup>2</sup> C read/write operations Single-byte read The master (or MCU) transmits a start condition (ST) to the FXOS8700CQ, followed by the slave address, with the R/W bit set to "0" for a write, and the FXOS8700CQ sends an acknowledgement. Then the master (or MCU) transmits the address of the register to read and the FXOS8700CQ sends an acknowledgement. The master (or MCU) transmits		
	a repeated start condition (SR), followed by the slave address with the R/W bit set to "1" for a read from the previously selected register. The FXOS8700CQ then acknowledges and transmits the data from the requested register. The master does not acknowledge (NAK) the transmitted data, but transmits a stop condition to end the data transfer. FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer, Data sheet: Technical data (Rev. 8 — 25 April 2017) at 15.		
	10.1.1 General I <sup>2</sup> C operation There are two signals associated with the I <sup>2</sup> C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. External pullup resistors connected to VDDIO are required for SDA and SCL. When the bus is free both the lines are high. The I <sup>2</sup> C interface is compliant with fast mode (400 kHz), and normal mode (100 kHz) I <sup>2</sup> C standards. Operation at frequencies higher than 400 kHz is possible, but depends on several factors including the pullup resistor values, and total bus capacitance (trace + device capacitance). See <u>Table 11</u> for more information.		
	FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer, Data sheet: Technical data (Rev. 8 — 25 April 2017) at 14.		

'474 Patent Claim	Representative NXP Product(s)		
	40.2.4 Convert SDI acception		
	10.2.1 General SPI operation		
	NOTE		
	FXOS8700CQ only supports a point-to-point SPI protocol, with only one master (MCU) and one slave device (FXOS8700CQ) present on the bus. FXOS8700CQ does not tri-state the MISO pin when the CS_B pin is deasserted (logic high), which can lead to a bus conflict if multiple slave devices are present on the bus.		
	Do not connect more than one master and one slave device on the SPI bus.		
	The CS_B pin is driven low at the start of a SPI transaction, held low for the duration of the transaction, and driven high after the transaction is complete. During a transaction the master toggles the SPI clock (SCLK) and transmits data on the MOSI pin.         FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer, Data sheet: Technical data (Rev. 8 — 25 April 2017) at 17.		
	Table 13. Serial interface pin descriptions		
	Pin name Pin description		
	VDDIO Digital interface power		
	SA1/CS_B I <sup>2</sup> C second least significant bit of device address/SPI chip select		
	SCL/SCLK I <sup>2</sup> C/SPI serial clock		
	SDA/MOSI I <sup>2</sup> C serial data/SPI master serial data out slave serial data in		
	SA0/MISO I <sup>2</sup> C least significant bit of the device address/SPI master serial data in slave out		
	FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer, Data sheet: Technical data (Rev. 8 — 25 April 2017) at 18.		



'474 Patent Claim		Representative NXP Product(s)
	7.4.1 I <sup>2</sup> C bit transmission	15
	The state of SDA when must be stable when S After the START signal Timing for the start cor	SCL is high determines the bit value being transmitted. SDA CL is high and change when SCL is low as shown in <u>Figure 14</u> . I has been transmitted by the master, the bus is considered busy. Indition is specified in <u>Table 105</u> .
	FXPS7115D4, Digital absolute pressure sensor, 40 kPa to 115 kPa, Product data sheet (Rev.	
	5uly 2020) at 15.	
	7.5 Standard 32-bit SF	'l protocol
	The device includes a si is a slave device and re- captured on the rising e- clock (CPHA = 0). The r completed through a se transmitted from the SP is transmitted from the si is not asserted. FXPS7115D4, Digital abso July 2020) at 17.	tandard SPI protocol requiring 32-bit data packets. The device quires that the base clock value be low (CPOL = 0) with data dge of the clock and data propagated on the falling edge of the most significant bit is transferred first (MSB first). SPI transfers are quence of two phases. During the first phase, the command is <u>1 master</u> to the device. During the second phase, response data slave device. MOSI and SCLK transitions are ignored when SS_B lute pressure sensor, 40 kPa to 115 kPa, Product data sheet (Rev. 4 — 17
	9 SCLK/SCL	In I <sup>2</sup> C mode, input pin 9 provides the serial clock. This pin must be connected to V <sub>CC</sub> with an external pull-up resistor, as shown in the application diagram. In SPI mode, input pin 9 provides the serial clock. An internal pull-down device is connected to this pin.
	10 MOSI	SPI data in In SPI mode, pin 10 functions as the serial data input to the SPI port. An internal pull-down device is connected to this pin.
	FXPS7115D4, Digital abso July 2020) at 4.	lute pressure sensor, 40 kPa to 115 kPa, Product data sheet (Rev. 4 — 17

'474 Patent Claim	Representative NXP Product(s)	
[1d.] wherein the slave serial interface is responsive to a read temperature command	In each of the Accused '474 Sensors, the slave serial interface is responsive to a read temperature command issued by the master serial interface to return a temperature value associated with the processor.	
issued by the master serial interface to return a temperature value associated with the processor.	For example, in each of the Accused '474 Sensors, the slave serial interface identified above is responsive to a read temperature command ( <i>e.g.</i> , the read temperature command directed to the TEMP_OUT register) issued by the identified master serial interface to return a temperature value ( <i>e.g.</i> , the temperature value in the TEMP_OUT register) associated with the processor. <i>See, e.g.</i> ,	
	<ul> <li>2 Features and benefits         <ul> <li>±2/4/8/16 g user-selectable, full-scale measurement ranges</li> <li>12-bit acceleration data</li> <li>8-bit temperature sensor data</li> <li>Low noise: 280 µg/√Hz in high performance mode</li> <li>Low power capability:</li> <li>≤ 1 µA I<sub>DD</sub> for ODRs up to 6.25 Hz</li> <li>&lt; 4 µA I<sub>DD</sub> for ODRs up to 50 Hz</li> </ul> </li> <li>FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 1.</li> </ul>	



'474 Patent Claim	Representative NXP Product(s)	
	10 I <sup>2</sup> C digital interface	
	The registers embedded within FXLS8962AF may be accessed using an $I^2C$ interface when the INTF_SEL pin is tied to GND. If the V <sub>DD</sub> supply is not present, the device will be in shutdown mode and any communications on the interface are ignored. When the device is on a common $I^2C$ -bus with other slave devices, the V <sub>DD</sub> supply pin must be left unconnected (high-impedance) when the device supply is turned off to ensure that the internal ESD protection diodes do not become forward biased and prevent the bus from functioning normally (clamping).	
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 16.	
	10.1.2 I <sup>2</sup> C read/write operations	
	10.1.2.1 Single byte read The master transmits a start condition (ST) to FXLS8962AF, followed by the slave address, with the R/W bit set to '0' for a write, and the FXLS8962AF sends an acknowledgement. Then the master transmits the address of the register to read and the FXLS8962AF sends an acknowledgement. The master transmits a repeated start condition (SR), followed by the slave address with the R/W bit set to '1' for a read from the previously selected register. The FXLS8962AF then acknowledges and transmits the data from the requested register. The master does not acknowledge (NAK) the transmitted data and then transmits a stop condition to end the data transfer.	
	10.1.2.2 Multiple byte read When performing a multi-byte or <i>burst</i> read, FXLS8962AF automatically increments the register read address pointer after a read command is received. Therefore, after following the steps of a single-byte read, multiple bytes of data can be read from sequential register addresses after each FXLS8962AF acknowledgment (ACK) is received until a no	
	acknowledge (NAK) is issued by the master followed by a stop condition (SP) signaling the end of the transfer.         FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18-19.	



'474 Patent Claim	Representative NXP Product(s)
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18- 20-21.
	11.3 SPI read operations with 4-wire mode A register read operation is initiated by transmitting a 1 for the R/W bit. Then, the 7- bit register read address, A[6:0] is encoded in the first byte. Following this first byte, a second byte of 0s or 1s (don't care condition) is transferred. After this transfer completes, the next 8 SCLK cycles (pulses 17 through 24) output the selected register content on the SPI_MISO line in MSb first order. The following figure shows the bus protocol for a single byte read operation.
	$SPI_{CS_B}$ $SCLK \_ /1 / 2 / 3 / 4 / 5 / 6 / 7 / 8 / 9 / 10 / 11 / 12 / 13 / 14 / 15 / 16 / 17 / 18 / 19 / 20 / 21 / 22 / 23 / 24$
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18- 21-22.

'474 Patent Claim	Representative NXP Product(s)
	Multiple-byte read operations are performed similarly to single-byte reads with additional bytes read out in multiples of eight SCLK cycles. The register read address is auto- incremented by FXLS8962AF so that every eighth clock edge will latch the address of the next sequential register read address. When the desired number of bytes has been read, a rising edge on SPI_CS_B terminates the transaction.
	SPLCS_B
	SCLK1\_2\3\4\5\6\7\6\9\10\11\12\13\14\15\16\17\18\18\20\21\22\23\24\25\28\27\20\29\30\31\32
	$\operatorname{SPL}_{\operatorname{MOSI}} \longrightarrow \operatorname{RW}(\operatorname{Ad})\operatorname{Ad}))))))))))))))))))))))))))))))))))))$
	SPI_MISO
	Figure 15. SPI multiple byte read protocol diagram (4-wire mode), R/W = 1
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18- 22.
	11.4 SPI read operations with 3-wire mode FXLS8962AF can be configured to operate in 3-wire software enabled SPI mode. In this mode, the SPI MISO pin is left unconnected and the SPI MOSI pin becomes a bidirectional input/output pin (SPI DATA). Read operations in 3-wire mode are the same as write operations in 3- and 4-wire modes, except that at the end of the address cycle (falling edge of clock pulse 16), the SPI_DATA pin automatically switches from an input to an output and with bit D7 as the current output state.
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18- 22.

'474 Patent Claim	Representative NXP Product(s)								
	SPI_0S_B								
Representative NXP Product(s)									
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	14.3 T	emperatu	re register	r					
	1431 T	EMD rogiet	or laddros	e (1v51)					
Table 50	E T o te o	ight-bit 2's co emperature o utput is only emperature so ne device to	omplement s lata is only v valid when N ensor is unc the next.	ensor tempe alid between /_CTRL_RE( alibrated and	ature value v –40 °C and ' 31[m_hms] > its output for	vith 0.96 °C/ 125 °C. The 0b00. Pleas a given tem	LSB sensitiv temperature se note that t perature will	vity. e sensor the I vary from	
Bit	7	6	5 pit alloca	4	3	2	1	0	
Symbol	1			die tempe	rature[7:0]	-		-	
Reset	0	0	0	0	0	0	0	0	
Access	R	R	R	R	R	R	R	R	
24	L.								
10.1.2 I <sup>2</sup> Si Th th ac re a fo aı	C read/wi ingle-byte he master ( e slave add cknowledge ad and the repeated s r a read fro nd transmit IAK) the tra	read or MCU) tra dress, with ement. The FXOS8700 tart condition the previous the data for posmitted do	tions ansmits a s the R/W bi in the maste DCQ sends on (SR), fol iously sele rom the ree	start conditi t set to "0" t er (or MCU an acknow llowed by th cted registe quested reg	on (ST) to t for a write, a transmits redgement is slave ado r. The FXC ister. The r	he FXOS8 and the FX the addres . The mast dress with S8700CQ naster doe	700CQ, fo OS8700C s of the reg ter (or MCL the R/W bi then ackn s not ackn	llowed by Q sends an gister to J) transmits it set to "1" owledges owledge	
	Table 50. Bit Symbol Reset Access FXOS870 Technical 10.1.2 I <sup>2</sup> Si Th th acc re a fo	14.3       T         14.3.1       T         14.3.1       T         14.3.1       T         10.1       TEMP register         Bit       7         Symbol       Reset         Reset       0         Access       R         FXOS8700CQ, 6-a:       Technical data (Rev         10.1.2       I²C read/wr         Single-byte       The master (         the slave add       acknowledge         read and the       a repeated s:         for a read fro       and transmits         (NAK) the training of the slave start of	14.3       Temperature         14.3.1       TEMP register         Eight-bit 2's contremperature of output is only temperature so one device to the temperature so temperature so the temperature so the temperature so	14.3 Temperature register         14.3.1 TEMP register (address         Eight-bit 2's complements         Temperature data is only v         output is only valid when N         temperature sensor is unc         one device to the next.         Table 50. TEMP register (address 0x51) bit alloca         Bit       7         Bit       7         Reset       0         Access       R         R       R         FXOS8700CQ, 6-axis sensor with int         Technical data (Rev. 8 — 25 April 20         10.1.2       I <sup>2</sup> C read/write operations         Single-byte read         The master (or MCU) transmits a sthe slave address, with the R/W bite acknowledgement. Then the master         read and the FXOS8700CQ sends a repeated start condition (SR), for for a read from the previously sele and transmits the data from the reperiously sele	14.3 Temperature register         14.3.1 TEMP register (address 0x51)         Eight-bit 2's complement sensor temperature data is only valid between output is only valid when M_CTRL_REC temperature sensor is uncalibrated and one device to the next.         Table 50. TEMP register (address 0x51) bit allocation         Bit       7       6       5       4         Symbol       die_tempe         Reset       0       0       0         Access       R       R       R         FXOS8700CQ, 6-axis sensor with integrated lint         Technical data (Rev. 8 — 25 April 2017) at 52.         10.1.2       I <sup>2</sup> C read/write operations         Single-byte read         The master (or MCU) transmits a start condition         the slave address, with the R/W bit set to "0" for acknowledgement. Then the master (or MCU)         read and the FXOS8700CQ sends an acknow         a repeated start condition (SR), followed by the for a read from the previously selected register and transmits the data from the requested registered registered register and transmits the data from th	14.3 Temperature register         14.3.1 TEMP register (address 0x51)         Eight-bit 2's complement sensor temperature value v Temperature data is only valid between -40 °C and °C output is only valid when M_CTRL_REG1[m_hms] > temperature sensor is uncalibrated and its output for one device to the next.         Table 50. TEMP register (address 0x51) bit allocation         Bit       7       6       5       4       3         Symbol         die_temperature[7:0]         Reset       0       0       0         Access         R       R       R         FXOS8700CQ, 6-axis sensor with integrated linear acce         Technical data (Rev. 8 — 25 April 2017) at 52.         10.1.2 I <sup>2</sup> C read/write operations         Single-byte read         The master (or MCU) transmits a start condition (ST) to t         the slave address, with the R/W bit set to "0" for a write, a acknowledgement. Then the master (or MCU) transmits a start condition (ST) to t         acknowledgement. Then the master (or MCU) transmits read and the FXOS8700CQ sends an acknowledgement a repeated start condition (SR), followed by the slave addres are address. The FXC and transmits the data from the requested register. The FXC and transmits the data from the requested register. The recompareaddition	14.3 Temperature register         14.3.1 TEMP register (address 0x51)         Eight-bit 2's complement sensor temperature value with 0.96 °C/ Temperature data is only valid between -40 °C and 125 °C. The output is only valid when M_CTRL_REG1[m_hms] > 0b00. Pleas temperature sensor is uncalibrated and its output for a given tem one device to the next.         Table 50. TEMP register (address 0x51) bit allocation         Bit       7       6       5       4       3       2         Symbol       die_temperature[7:0]         Reset       0       0       0       0         Access       R       R       R       R         FXOS8700CQ, 6-axis sensor with integrated linear accelerometer         Technical data (Rev. 8       25 April 2017) at 52.         10.1.2 I <sup>2</sup> C read/write operations         Single-byte read         The master (or MCU) transmits a start condition (ST) to the FXOS8 the slave address, with the R/W bit set to "0" for a write, and the FX acknowledgement. Then the master (or MCU) transmits the address read and the FXOS8700CQ sends an acknowledgement. The mast a repeated start condition (SR), followed by the slave address with for a read from the previously selected register. The FXOS8700CQ and transmits the data from the requested register. The master doe	14.3 Temperature register         14.3.1 TEMP register (address 0x51)         Eight-bit 2's complement sensor temperature value with 0.96 °C/LSB sensitives Temperature data is only valid between -40 °C and 125 °C. The temperature output is only valid when M_CTRL_REG1[m_hms] > 0b00. Please note that it temperature sensor is uncalibrated and its output for a given temperature will one device to the next.         Table 50. TEMP register (address 0x51) bit allocation         Bit       7       6       5       4       3       2       1         Symbol       die_temperature[7:0]       Reset       0       0       0       0       0         Reset       0       0       0       0       0       0       0         Access       R       R       R       R       R       R         FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and mathematical data (Rev. 8 — 25 April 2017) at 52.       10.1.2       I <sup>2</sup> C read/write operations         Single-byte read       The master (or MCU) transmits a start condition (ST) to the FXOS8700CQ, for the slave address, with the R/W bit set to "0" for a write, and the FXOS8700CQ, for the slave address, with the R/W bit set to "0" for a write, and the FXOS8700CQ sends an acknowledgement. The master (or MCU) a repeated start condition (SR), followed by the slave address of the read read and the FXOS8700CQ sends an acknowledgement. The master (or MCU) a repeated start condition (SR), followed by the slave address with	14.3 Temperature register         14.3.1 TEMP register (address 0x51)         Eight-bit 2's complement sensor temperature value with 0.96 *C/LSB sensitivity. Temperature data is only valid between -40 *C and 125 *C. The temperature sensor output is only valid when M_CTRL_REG1[m_hms] > 0b00. Please note that the temperature sensor is uncalibrated and its output for a given temperature will vary from one device to the next.         Table 50. TEMP register (address 0x51) bit allocation         Bit       7       6       5       4       3       2       1       0         Symbol       die_temperature[7:0]       Reset       0       0       0       0       0         Access       R       R       R       R       R       R       R         FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer Technical data (Rev. 8 — 25 April 2017) at 52.       10.1.2       I²C read/write operations         Single-byte read       The master (or MCU) transmits a start condition (ST) to the FXOS8700CQ, followed by the slave address, with the R/W bit set to "0" for a write, and the FXOS8700CQ sends an acknowledgement. Then the master (or MCU) transmits the address of the register to read and the FXOS8700CQ sends an acknowledgement. The master (or MCU) transmits a repeated start condition (SR), followed by the slave address with the R/W bit set to "1" for a read from the previously selected register. The FXOS8700CQ then acknowledges and transmits the data from the requested register. The master does not acknowledge

'474 Patent Claim	Representative NXP Product(s)							
	FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer, Data sheet: Technical data (Rev. 8 — 25 April 2017) at 15.							
	< Single-byte read >							
	Master     ST     Device address[6:0]     W     Register address[7:0]     SR     Device address[6:0]     R     NAK     SP							
	Slave AK AK AK Data[7:0]							
	< Multiple-byte read >							
	Master         ST         Device address[6:0]         W         Register address[7:0]         SR         Device address[6:0]         R         AK							
	Slave AK AK AK Data[7:0]							
	Master AK AK NAK SP							
	Slave         Data[7:0]         Data[7:0]         Data[7:0]							
	FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer, Data sheet: Technical data (Rev. 8 — 25 April 2017) at 16.							
	10.2.2 SPI read/write operations							
	A read operation is initiated by transmitting a 0 for the R/W bit. Then the 8-bit register							
	address, ADDR[7:0] is encoded in the first and second serialized bytes. Subsequent bits							
	are ignored by the part. The read data is deserialized from the MISO pin.							
	FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer, Data sheet:							
	rechnical data (Kev. $\delta - 25$ April 2017) at 18.							

'474 Patent Claim	Representative NXP Product(s)	
	1 General description	
	The FXPS7115D4 high-performance, high-precision barometric absolute pressure (BAP) sensor consists of a compact capacitive micro-electro-mechanical systems (MEMS) device coupled with a digital integrated circuit (IC) producing a fully calibrated digital output.	
	The sensor is based on NXP's high-precision capacitive pressure cell technology. The architecture benefits from redundant pressure transducers as an expanded quality measure. This sensor delivers highly accurate pressure and temperature readings through either a serial peripheral interface (SPI) or an inter-integrated circuit ( $I^2C$ ) interface. The FXPS7115D4 uses either a 3.3 V or 5.0 V power supply. Furthermore, the sensor employs an on-demand digital self-test for the digital IC and the MEMS transducers.	
	FXPS7115D4, Digital absolute pressure sensor, 40 kPa to 115 kPa, Product data sheet (Rev. 4 July 2020) at 1.	— 17

'474 Patent Claim			Representativ	e NXP Product(s)	
	7.3.4	Temperature senso	r		
	7244	<b>T</b>			
	1.3.4.1	remperature sensor s	signal chain		
		The device includes a t <u>Figure 12</u> shows a simple specified in <u>Table 104</u> a	emperature sensor for signa olified block diagram. Tempe and <u>Table 105</u> .	al compensation and user readabili erature sensor parameters are	ty.
		temperature sensor CO		VING RAGE AND GAIN TRIM	
		Figure 12. Temperatur	e sensor signal chain block d	liagram	0
	7.3.4.2	Temperature sensor of	output scaling equation		
		Equation 5 is used to c Table 8.	onvert temperature readings	with the variables specified in	
			$T_{DEGC} = \frac{T_{LSB} - T0_{LS}}{T_{SENSE}}$	<u>u</u>	(5)
		where:			
		T <sub>DEGC</sub> = The tempe T <sub>LSB</sub> = The tempera	rature output in degrees C ture output in LSB		
		TO <sub>LSB</sub> = The expect	ed temperature output in LS	Bat0°C	
		T <sub>SENSE</sub> = The expect	ted temperature sensitivity i	n LSB/°C	
		Table 8. Temperature c	onversion variables	11	
		Data reading	TOLSB (LSB)	TBENDE LSB/C)	
	1	8-bit register read	68	1	

'474 Patent Claim					F	Represe	entativ	e NXP	Produ	ct(s)			
	7.6 User-accessible data array												
			A u of a proj inco	ser-access one time p grammable orporate inc	ible data ar programma block, and dependent of	ray allows ble (OTP) read-only data verific	each devid factory-pro registers fi ation.	ce to be cu grammable or data and	stomized. 1 e block, an d device sta	The array of OTP user- itus. The C	onsists		
	Table 3	3. User-access	sible	data — sen	sor specific	informatio	n						
	Address	Register	Туре	tu)			B	34t					
				7	6	5	4	3	2	1	0		
	General	device Information		1			0018						
	01h	DEVSTAT	R	DSP ERR	reserved	COMM ERR	MEMTEMP	SUPPLY	TESTMODE	DEVRES	DEVINIT		
			1372				ERR	ERR			a second a s		
	02h	DEVSTAT1	R	VCCUV_	reserved	VCCOV_	reserved	INTREGA_	INTREG_ ERR	INTREGF_	CONT_ERR		
	03h	DEVSTAT2	R	F_OTP_ERR	U_OTP_ ERR	U_RW_ERR	U_W_ ACTIVE	reserved	TEMP0_ ERR	reserved	reserved		
	04h	DEVSTAT3	R	MISO_ERR	OSCTRAIN_ ERR	reserved	reserved	reserved	reserved	reserved	reserved		
	05h	reserved	R				rese	erved					
	O6h to ODh	reserved	R	reserved									
	DEh	TEMPERATURE	R				TEM	P[7:0]					
	OFn	reserved	R				rese	erved					

	Representative NXP Product(s)
	Representative NXP Product(s)         7.4.6.2 Register read transfers         The device supports I <sup>2</sup> C register read data transfers. Register read data transfers are constructed as follows:         1. The master transmits a START condition.       2. The master transmits the 7-bit slave address.         3. The master transmits a '0' for the read/write bit to indicate a write operation.       4. The slave transmits an ACK.         5. The master transmits the register address to be read.       6. The slave transmits an ACK.         7. The master transmits a repeat START condition.       8. The master transmits the 7-bit slave address.         9. The master transmits the 7-bit slave address.       9. The master transmits a '1' for the read/write bit to indicate a read operation.
F	<ul> <li>8. The master transmits the 7-bit slave address.</li> <li>9. The master transmits a '1' for the read/write bit to indicate a read operation.</li> <li>10. The slave transmits an ACK.</li> <li>11. The slave transmits the data from the register addressed.</li> <li>12. The master transmits a NACK.</li> <li>13. The master transmits a STOP condition.</li> </ul>

'474 Patent Claim	Representative NXP Product(s)						
	7.5.3	Command summary					
	7.5.3.1	Register read command					
		The device supports a register read command. The register read command uses the upper 7 bits of the addresses defined in <u>Section 7.6 "User-accessible data array"</u> to address 8-bit registers in the register map.					
		The response to a register read command is shown in <u>Section 7.5.3.1.2 "Register read</u> <u>response message format"</u> . The response is transmitted on the next SPI message if and only if all of the following conditions are met:					
		<ul> <li>No SPI error is detected (see Section 7.5.5.3 "SPI error")</li> <li>No MISO error is detected (see Section 7.5.5.4 "SPI data output verification error")</li> </ul>					
		If these conditions are met, the device responds to the register read request as shown in <u>Section 7.5.3.1.2 "Register read response message format"</u> . Otherwise, the device responds with the error response as defined in <u>Section 7.5.5.2 "Detailed status field"</u> . The register read response includes the register contents at the rising edge of SS_B for the register read command.					
	FXPS71 July 202	15D4, Digital absolute pressure sensor, 40 kPa to 115 kPa, Product data sheet (Rev. 4 — 17 0) at 20.					

+ Patent Claim	Representative NXP Product(s)							
	7.5.3	]						
	Table 13. Registe							
	MSB: bit 31; LSB:	bit O	and the					
	31 30 29 28 27	26 25	24 23	22 21 20 19 18 17	16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
				Regis	ter access	command		
	Command I C[3:0]	Fixed bits must = 0h	s: h	Register address		Register data	8-bit CRC	
	1 1 0 0 0	0 0	0	RA[7:1]	RA[0]	0 0 0 0 0 0 0 0	CRC[7:0]	
		T	Table 14 Bit field	. Register read com	mand me Definition	essage bit field descriptions		
		(	C[3:0]		Register re	ad command = '1100'		
		F	RA[7:0]		RA[7:1] co	ntains the word address of the register	to be read.	
		4	CRC[7:0]		Read CRC	Section		
				Regis	ter access	command		
	Command I C[0], [3:1] S	Basic Status	Unused Data 0h	Register data: conter of RA[7:1] high byt	nts e	Register data: contents of RA[7:1] low byte	8-bit CRC	
	Command C[0], [3:1]         H           0         1         1         0         S	Basic Status ST[1:0]	Unused Data 0h 0 0	Register data: conter of RA[7:1] high byt RD[15:8]	nts e	Register data: contents of RA[7:1] low byte RD[7:0]	8-bit CRC CRC[7:0]	
	Command C[0], [3:1]         I           0         1         1         0         S           FXPS7115D4         July 2020) at         Table 16. R         Bit field	Basic Status ST[1:0] 4, Dig 20.	Unused Data 0h 0 0 gital a	Register data: conter of RA[7:1] high byt RD[15:8] absolute presso response messa Definition	ure se	Register data: contents of RA[7:1] low byte RD[7:0] ensor, 40 kPa to 115 field descriptions	8-bit CRC CRC[7:0]	] sheet (Rev. 4 –
	Command C[0], [3:1]         I           0         1         1         0         S           FXPS7115D4         July 2020) at         Table 16. R         Bit field           C[0], [3:1]         C[0], [3:1]         C[0], [3:1]         C[0], [3:1]	Basic Status ST[1:0] 4, Dig 20.	Unused Data 0h 0 0 gital a er read	Register data: conter of RA[7:1] high byt RD[15:8] absolute pressa response messa Definition Register Read Comman	ure se	Register data: contents of RA[7:1] low byte RD[7:0] ensor, 40 kPa to 115 field descriptions	8-bit CRC CRC[7:0]	sheet (Rev. 4 –
	Command C[0], [3:1]         I           0         1         1         0         S           FXPS7115D4         July 2020) at         Table 16. R         Bit field           C[0], [3:1]         ST[1:0]         ST[1:0]         ST[1:0]	Basic Status ST[1:0] 4, Dig 20.	Unused Data 0h 0 0 gital a er read F F	Register data: conter of RA[7:1] high byt RD[15:8] absolute press response messa Definition Register Read Comman Status	ure se	Register data: contents of RA[7:1] low byte RD[7:0] ensor, 40 kPa to 115 field descriptions	8-bit CRC CRC[7:0]	] sheet (Rev. 4 –
	Command C[0], [3:1]         I           0         1         1         0         s           FXPS7115D4         July 2020) at         Table 16. R         Bit field         C[0], [3:1]           ST[1:0]         RD[15:8]         RD[15:8]         RD[15:8]         R	Basic Status ST[1:0] 4, Dig 20.	Unused Data 0h 0 0 gital a er read F 5 5 1	Register data: conter of RA[7:1] high byt RD[15:8] absolute pression response messa Definition Register Read Comman Status The contents of the register	ure se age bit d = '0110	Register data: contents of RA[7:1] low byte RD[7:0] ensor, 40 kPa to 115 field descriptions	8-bit CRC CRC[7:0] 5 kPa, Product data	] sheet (Rev. 4 –
	Command C[0], [3:1]         I           0         1         1         0         S           FXPS7115D4         July 2020) at         Table 16. R         R           Bit field         C[0], [3:1]         ST[1:0]         RD[15:8]         RD[7:0]	Basic Status ST[1:0] 4, Dig 20.	Unused Data 0h 0 0 gital a er read F F 5 5 1	Register data: conter of RA[7:1] high byt RD[15:8] absolute pression response messa Definition Register Read Comman Status The contents of the regist The contents of the regist	ure se age bit d = '0110 ster addre	Register data: contents of RA[7:1] low byte RD[7:0] ensor, 40 kPa to 111 field descriptions	8-bit CRC CRC[7:0] 5 kPa, Product data 0] = 1) ] = 0)	sheet (Rev. 4 –
	Command C[0], [3:1]         I           0         1         1         0         S           FXPS7115D4         July 2020) at         Table 16. R         R           Bit field         C[0], [3:1]         ST[1:0]         RD[15:8]           RD[7:0]         CRC[7:0]         CRC[7:0]         CRC[7:0]	Basic Status ST[1:0] 4, Dig 20.	Unused Data 0h 0 0 gital : er read 6 F F S S 1 1 1 8	Register data: conter of RA[7:1] high byt RD[15:8] absolute pressa perinition Register Read Comman Status The contents of the regist Hoit CRC	nts e ure se nge bit d = '0110 ster addre	Register data: contents of RA[7:1] low byte RD[7:0] ensor, 40 kPa to 115 field descriptions	8-bit CRC CRC[7:0] 5 kPa, Product data 0] = 1) ] = 0)	] sheet (Rev. 4 -

'474 Patent Claim	Representative NXP Product(s)
[8a.]. A method for communicating over a point to point serial	To the extent the preamble is limiting, the Accused '474 Sensors perform a method for communicating over a point to point serial communication system having a clock signal line and a data signal line coupling a serial interface master and a serial interface slave.
having a clock signal line and a data signal line coupling a serial interface master and a serial interface slave, the method comprising:	For example, each of the Accused '474 Sensors perform a method for communicating over a point to point serial communication system (e.g., system identified below) having a clock signal line ( <i>e.g.</i> , the serial clock line (SCL) and/or the SPI clock (SCLK)) and a data signal line ( <i>e.g.</i> , the serial data line (SDA) and/or the SPI master serial data out slave serial data in (MOSI)) coupling a serial interface master ( <i>e.g.</i> , the SPI/I2C interface on the master/MCU and/or the host processor) and a serial interface slave ( <i>e.g.</i> , SPI/I2C).
	See, e.g.,
	https://www.avnet.com/shop/us/products/nxp/fxos8700cqr1- 3074457345626313537?fromPage=autoSuggest&langId=-1&autoSuggestSearchTerm=FXOS















'474 Patent Claim	Representative NXP Product(s)
	10.1.2 I <sup>2</sup> C read/write operations
	The master transmits a start condition (ST) to FXLS8962AF, followed by the slave address, with the R/W bit set to '0' for a write, and the FXLS8962AF sends an acknowledgement. Then the master transmits the address of the register to read and the FXLS8962AF sends an acknowledgement. The master transmits a repeated start condition (SR), followed by the slave address with the R/W bit set to '1' for a read from the previously selected register. The FXLS8962AF then acknowledges and transmits the data from the requested register. The master does not acknowledge (NAK) the transmitted data and then transmits a stop condition to end the data transfer.
	<ul> <li>FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18.</li> <li><b>11 SPI interface</b></li> </ul>
	The SPI interface is a classical <u>Master/Slave serial port</u> . FXLS8962AF is always considered to be the slave device and thus never initiates communication with the host processor.
	The SPI interface of FXLS8962AF is compatible with interface mode 00, corresponding to CPOL = 0 and CPHA = 0.
	For CPOL = 0, the idle value of the clock is zero, and the active value of the clock is 1. For CPHA = 0, data is captured on the clock's rising edge (low to high transition) and data is propagated on the clock's falling edge (high to low transition).
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 20.
	10.1.1 General I <sup>2</sup> C operation There are two signals associated with the I <sup>2</sup> C-bus: the Serial Clock Line (SCL) and the Serial Data line (SDA). SDA is a bidirectional signal used for sending and receiving the data to/from the interface. External pull-up resistors connected to V <sub>DD</sub> are required for SDA and SCL. When the I <sup>2</sup> C-bus is free, SCL and SDA are high.

'474 Patent Claim	Representative NXP Product(s)
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18.
	11.1 General SPI operation         The SPI_CS_B pin is driven low at the start of a transaction, held low for the duration of the transfer, and then driven high again after the transaction is completed. During a transaction, the master toggles the clock (SCLK). The SCLK polarity is defined as having an idle value that is low, and an active phase that is high (CPOL = 0). Serial input and output data is captured on the clock's rising edge and propagated on the falling edge         EXI S8962AE       3-Axis Low-g Accelerometer. Product data sheet (Rev. 5.3 — 10 December 2019) at 20
	<ul> <li>11.4 SPI read operations with 3-wire mode</li> <li>FXLS8962AF can be configured to operate in 3-wire software enabled SPI mode. In this mode, the SPI_MISO pin is left unconnected and the SPI_MOSI pin becomes a bidirectional input/output pin (SPI_DATA). Read operations in 3-wire mode are the same as write operations in 3- and 4-wire modes, except that at the end of the address cycle (falling edge of clock pulse 16), the SPI_DATA pin automatically switches from an input to an output and with bit D7 as the current output state.</li> <li>FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 22.</li> </ul>

'474 Patent Claim	Representative NXP Product(s)							
	SDA / SPI_MOSI / SPI_DATA	4	<ul> <li>Mode dependent Multifunction serial interface pin.<sup>[2]</sup></li> <li>INTF_SEL = V<sub>DD</sub>:</li> <li>SPI_MOSI: In 4-wire SPI mode this pin functions as the serial data input (Master Out Slave In).</li> <li>SPI_DATA<sup>[3]</sup>: In 3-wire SPI mode this pin functions as the bidirectional serial data input/output.</li> <li>INTF_SEL = GND:</li> <li>SDA: This pin functions as the I<sup>2</sup>C Serial Data input/output.</li> </ul>					
	SCL / SCLK	5	Mode dependent Multifunction serial interface pin. <sup>[2]</sup> INTF_SEL = V <sub>DD</sub> : • SPI serial clock input (3- and 4-wire modes) INTF_SEL = GND: • I <sup>2</sup> C serial clock input					
	FXLS8962AF, 3-Axis Lo	w-g Ac	ccelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 4.					



'474 Patent Claim	Representative NXP Product(s)
	10.1.2 I <sup>2</sup> C read/write operations Single-byte read
	The master (or MCU) transmits a start condition (ST) to the FXOS8700CQ, followed by the slave address, with the R/W bit set to "0" for a write, and the FXOS8700CQ sends an acknowledgement. Then the master (or MCU) transmits the address of the register to read and the FXOS8700CQ sends an acknowledgement. The master (or MCU) transmits a repeated start condition (SR), followed by the slave address with the R/W bit set to "1" for a read from the previously selected register. The FXOS8700CQ then acknowledges and transmits the data from the requested register. The master does not acknowledge (NAK) the transmitted data, but transmits a stop condition to end the data transfer.
	FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer, Data sheet: Technical data (Rev. 8 — 25 April 2017) at 15.
	There are two signals associated with the I <sup>2</sup> C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. External pullup resistors connected to VDDIO are required for SDA and SCL. When the bus is free both the lines are high. The I <sup>2</sup> C interface is compliant with fast mode (400 kHz), and normal mode (100 kHz) I <sup>2</sup> C standards. Operation at frequencies higher than 400 kHz is possible, but depends on several factors including the pullup resistor values, and total bus capacitance (trace + device capacitance). See <u>Table 11</u> for more information.
	FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer, Data sheet: Technical data (Rev. 8 — 25 April 2017) at 14.

'474 Patent Claim	Representative NXP Product(s)
	40.2.4 Convert SDI acception
	10.2.1 General SPI operation
	NOTE
	FXOS8700CQ only supports a point-to-point SPI protocol, with only one master (MCU) and one slave device (FXOS8700CQ) present on the bus. FXOS8700CQ does not tri-state the MISO pin when the CS_B pin is deasserted (logic high), which can lead to a bus conflict if multiple slave devices are present on the bus.
	Do not connect more than one master and one slave device on the SPI bus.
	The CS_B pin is driven low at the start of a SPI transaction, held low for the duration of the transaction, and driven high after the transaction is complete. During a transaction the master toggles the SPI clock (SCLK) and transmits data on the MOSI pin.         FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer, Data sheet: Technical data (Rev. 8 — 25 April 2017) at 17.
	Table 13. Serial interface pin descriptions
	Pin name Pin description
	VDDIO Digital interface power
	SA1/CS_B I <sup>2</sup> C second least significant bit of device address/SPI chip select
	SCL/SCLK I <sup>2</sup> C/SPI serial clock
	SDA/MOSI I <sup>2</sup> C serial data/SPI master serial data out slave serial data in
	SA0/MISO I <sup>2</sup> C least significant bit of the device address/SPI master serial data in slave out
	FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer, Data sheet: Technical data (Rev. 8 — 25 April 2017) at 18.

![](_page_58_Figure_0.jpeg)

'474 Patent Claim			Representative NXP Product(s)
	7.4.1 I <sup>2</sup> C	bit transmission	ns
	mu: Afte	state of SDA when st be stable when S er the START signa ning for the start cor	SCL is high and change when SCL is low as shown in <u>Figure 14</u> . I has been transmitted by the master, the bus is considered busy. Indition is specified in <u>Table 105</u> .
	FXPS7115 July 2020)	D4, Digital abso at 13.	lute pressure sensor, 40 kPa to 115 kPa, Product data sheet (Rev. 4 — 17
	7.5 Star	ndard 32-bit SF	PI protocol
	The dis a since the complexity of the complexity	device includes a salave device and re salave device and re ured on the rising e (CPHA = 0). The bleted through a se smitted from the SF nsmitted from the st t asserted. D4, Digital abso	standard SPI protocol requiring 32-bit data packets. The device equires that the base clock value be low (CPOL = 0) with data edge of the clock and data propagated on the falling edge of the most significant bit is transferred first (MSB first). SPI transfers are equence of two phases. During the first phase, the command is PI master to the device. During the second phase, response data slave device. MOSI and SCLK transitions are ignored when SS_B
	July 2020)	at 17.	
	9	SCLK/SCL	In I <sup>2</sup> C mode, input pin 9 provides the serial clock. This pin must be connected to V <sub>CC</sub> with an external pull-up resistor, as shown in the application diagram. In SPI mode, input pin 9 provides the serial clock. An internal pull-down device is connected to this pin.
	10	MOSI	SPI data in In SPI mode, pin 10 functions as the serial data input to the SPI port. An internal pull-down device is connected to this pin.
	FXPS7115 July 2020)	D4, Digital abso at 4.	ulute pressure sensor, 40 kPa to 115 kPa, Product data sheet (Rev. 4 — 17
[8b.] sending a read	The Accus	ed '474 Sensors	performs a step of sending a read temperature command to the serial

'474 Patent Claim	Representative NXP Product(s)
temperature command to	interface slave from the serial interface master using the clock signal line and the data signal line.
from the serial interface master using the clock signal line and the data signal line; and	For example, each of the Accused '474 Sensors perform a step of sending a read temperature command ( <i>e.g.</i> , the read temperature command directed to the TEMP_OUT register) to the serial interface slave identified above from the serial interface master identified above using the clock signal line identified above and the data signal line identified above.
	<ul> <li>2 Features and benefits         <ul> <li>±2/4/8/16 g user-selectable, full-scale measurement ranges</li> <li>12-bit acceleration data</li> <li>8-bit temperature sensor data</li> <li>Low noise: 280 µg/√Hz in high performance mode</li> <li>Low power capability:</li> <li>≤ 1 µA I<sub>DD</sub> for ODRs up to 6.25 Hz</li> <li>&lt; 4 µA I<sub>DD</sub> for ODRs up to 50 Hz</li> </ul> </li> <li>FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 1.</li> </ul>

![](_page_61_Figure_0.jpeg)

'474 Patent Claim	Representative NXP Product(s)
	10 I <sup>2</sup> C digital interface
	The registers embedded within FXLS8962AF may be accessed using an $I^2C$ interface when the INTF_SEL pin is tied to GND. If the V <sub>DD</sub> supply is not present, the device will be in shutdown mode and any communications on the interface are ignored. When the device is on a common $I^2C$ -bus with other slave devices, the V <sub>DD</sub> supply pin must be left unconnected (high-impedance) when the device supply is turned off to ensure that the internal ESD protection diodes do not become forward biased and prevent the bus from functioning normally (clamping).
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 16.
	10.1.2 I <sup>2</sup> C read/write operations
	10.1.2.1 Single byte read
	The master transmits a start condition (ST) to FXLS8962AF, followed by the slave address, with the R/W bit set to '0' for a write, and the FXLS8962AF sends an acknowledgement. Then the master transmits the address of the register to read and the FXLS8962AF sends an acknowledgement. The master transmits a repeated start condition (SR), followed by the slave address with the R/W bit set to '1' for a read from the previously selected register. The FXLS8962AF then acknowledges and transmits the data from the requested register. The master does not acknowledge (NAK) the transmitted data and then transmits a stop condition to end the data transfer.
	10.1.2.2 Multiple byte read
	When performing a multi-byte or <i>burst</i> read, FXLS8962AF automatically increments the register read address pointer after a read command is received. Therefore, after following
	the steps of a single-byte read, multiple bytes of data can be read from sequential register addresses after each FXLS8962AF acknowledgment (ACK) is received until a no acknowledge (NAK) is issued by the master followed by a stop condition (SP) signaling the end of the transfer.
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18- 19.

![](_page_63_Figure_0.jpeg)

'474 Patent Claim	Representative NXP Product(s)
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18- 20-21.
	11.3 SPI read operations with 4-wire mode A register read operation is initiated by transmitting a 1 for the R/W bit. Then, the 7- bit register read address, A[6:0] is encoded in the first byte. Following this first byte, a second byte of 0s or 1s (don't care condition) is transferred. After this transfer completes, the next 8 SCLK cycles (pulses 17 through 24) output the selected register content on the SPI_MISO line in MSb first order. The following figure shows the bus protocol for a single byte read operation.
	$SPI_{CS_B}$ $SCLK \_ 1 \sqrt{2} \sqrt{3} \sqrt{4} \sqrt{5} \sqrt{6} \sqrt{7} \sqrt{8} \sqrt{9} \sqrt{10} \sqrt{11} \sqrt{12} \sqrt{13} \sqrt{14} \sqrt{15} \sqrt{16} \sqrt{17} \sqrt{18} \sqrt{19} \sqrt{20} \sqrt{21} \sqrt{22} \sqrt{23} \sqrt{24}$ $SPI_{MOSI} = -\frac{RW}{A6} \sqrt{A6} \sqrt{A5} \sqrt{A4} \sqrt{A3} \sqrt{A2} \sqrt{A1} \sqrt{A0} \sqrt{X} \sqrt{X} \sqrt{X} \sqrt{X} \sqrt{X} \sqrt{X} \sqrt{X} X$
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18- 21-22.

'474 Patent Claim	Representative NXP Product(s)
	Multiple-byte read operations are performed similarly to single-byte reads with additional bytes read out in multiples of eight SCLK cycles. The register read address is auto- incremented by FXLS8962AF so that every eighth clock edge will latch the address of the next sequential register read address. When the desired number of bytes has been read, a rising edge on SPI_CS_B terminates the transaction.
	SPLCS_B
	SCLK1 2 3 4 5 6 7 7 6 1 6 1 7 1 2 1 3 1 4 1 5 1 6 1 7 1 8 1 6 20 2 1 2 2 2 2 2 4 2 6 2 7 2 9 2 9 2 9 3 1 5 2
	$spl_Mosi = - RW(Ab(Ab(Ab(Ab(Ab(Ab(X)(Ab(X)(X$
	SPI_MISO
	Figure 15. SPI multiple byte read protocol diagram (4-wire mode), R/W = 1
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18- 22.
	11.4 SPI read operations with 3-wire mode FXLS8962AF can be configured to operate in 3-wire software enabled SPI mode. In this mode, the SPI MISO pin is left unconnected and the SPI MOSI pin becomes a bidimeticated introduction (SPI DATA). Deed competition in 2-wire mode and the
	bidirectional input/output pin (SPI_DATA). Read operations in 3-wire mode are the same as write operations in 3- and 4-wire modes, except that at the end of the address cycle (falling edge of clock pulse 16), the SPI_DATA pin automatically switches from an input to an output and with bit D7 as the current output state.
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18- 22.

'474 Patent Claim	Representative NXP Product(s)
	$[SPL_GS_B] = [SCLK \_ (\sqrt{2}\sqrt{3}\sqrt{4}\sqrt{5}\sqrt{6}\sqrt{7}\sqrt{8}\sqrt{9}\sqrt{6}\sqrt{1}\sqrt{12}\sqrt{13}\sqrt{4}\sqrt{15}\sqrt{16}\sqrt{19}\sqrt{19}\sqrt{19}\sqrt{20}\sqrt{21}\sqrt{22}\sqrt{21}\sqrt{24}\sqrt{24}\sqrt{24}\sqrt{24}\sqrt{24}\sqrt{24}\sqrt{24}24$

	14.3 Te								
		emperatur	re register	rij					
	1431 T	EMP regist	er (addres	s (1x51)					
14.5.1 TEMP TEUSIER (dutress 0x51)									
Eight-bit 2's complement sensor temperature value with 0.96 °C/LSB sensitivity. Temperature data is only valid between -40 °C and 125 °C. The temperature sensor output is only valid when M_CTRL_REG1[m_hms] > 0b00. Please note that the temperature sensor is uncalibrated and its output for a given temperature will vary from one device to the next.									
Table 50.	TEMP register	(address 0x!	51) bit allocat	tion					
Bit	7	6	5	4	3	2	/1	0	
Symbol				die_tempe	rature[7:0]				
Reset	0	0	0	0	0	0	0	0	
Access	R	R	R	R	R	R	R	R	
10.1.2 I <sup>2</sup> Si Th th ac re a fo ar (N W th fo se ac	C read/wr ingle-byte i he master (d e slave add cknowledge ad and the repeated st r a read fro nd transmits IAK) the tra /hen perform e register a llowing the equential reg cknowledge	ite operat read or MCU) tra ress, with ment. Ther FXOS8700 art condition atte data for nsmitted data ddress rea steps of a gisters afte (NAK) occ	tions ansmits a s the R/W bin in the mastro DCQ sends on (SR), fol iously sele rom the rec ata, but tra i-byte or "b d pointer a single-byte r each FXC urs from th	etart conditi t set to "0" f er (or MCU an acknow lowed by th cted registe quested reg nsmits a st urst" read, fter a read read, mult DS8700CQ e master fo	on (ST) to t or a write, a transmits t ledgement e slave add r. The FXC ister. The r op condition the FXOS8 command i ple bytes o acknowled llowed by a	he FXOS8 and the FX he addres . The mast dress with S8700CQ naster doe n to end the 700CQ aut s received f data can gment (AK stop cond	700CQ, fo COS8700C s of the reg ter (or MCU the R/W bi then ackn s not ackn s not ackn e data tran tomatically . Therefore be read fro ) is receive lition (SP) s	llowed by Q sends an gister to J) transmits it set to "1" owledges owledge isfer. increments e, after om ed until a no signaling an	
	Table 50.         Bit         Symbol         Reset         Accesss         FXOS870         Technical         10.1.2       I²         Si         Ti         th         access         V         th         access	Table 50. TEMP register Bit 7 Symbol Reset 0 Access R FXOS8700CQ, 6-ax Technical data (Rev 10.1.2 I <sup>2</sup> C read/wr Single-byte r The master (of the slave add acknowledge read and the a repeated st for a read from and transmits (NAK) the tra When perform the register a following the sequential regi acknowledge	Temperature of output is only temperature so one device to a so o	Temperature data is only v         output is only valid when M         temperature sensor is uncoordevice to the next.         Table 50. TEMP register (address 0x51) bit allocal         Bit       7       6       5         Symbol       R       R       R         Reset       0       0       0       0         Access       R       R       R       R         FXOS8700CQ, 6-axis sensor with int       Technical data (Rev. 8 — 25 April 20)         10.1.2 I <sup>2</sup> C read/write operations         Single-byte read         The master (or MCU) transmits a sthe slave address, with the R/W bi         acknowledgement. Then the master         read and the FXOS8700CQ sends         a repeated start condition (SR), fol         for a read from the previously sele         and transmits the data from the read         When performing a multi-byte or "b         When performing a multi-byte or "b         the register address read pointer a       following the steps of a single-byte       sequential registers after each FXO	Temperature data is only valid between output is only valid when M_CTRL_REC temperature sensor is uncalibrated and one device to the next.         Table 50. TEMP register (address 0x51) bit allocation         Bit       7       6       5       4         Symbol       die_temperature       Reset       0       0       0         Reset       0       0       0       0       0         Access       R       R       R       R         FXOS8700CQ, 6-axis sensor with integrated lint       Technical data (Rev. 8 — 25 April 2017) at 52.         10.1.2 I <sup>2</sup> C read/write operations         Single-byte read         The master (or MCU) transmits a start condition the slave address, with the R/W bit set to "0" for acknowledgement. Then the master (or MCU) read and the FXOS8700CQ sends an acknow a repeated start condition (SR), followed by the for a read from the previously selected register and transmits the data from the requested reg (NAK) the transmitted data, but transmits a start condition (SR), followed by the for a read from the previously selected register and transmits the data from the requested reg (NAK) the transmitted data, but transmits a start condition following the steps of a single-byte read, multi sequential registers after each FXOS8700CQ acknowledge (NAK) occurs from the master for the following the steps of a single-byte read, multi sequential registers after eac	Temperature data is only valid between -40 °C and 1 output is only valid when M_CTRL_REG1[m_hms] > temperature sensor is uncalibrated and its output for one device to the next.         Table 50.       TEMP register (address 0x51) bit allocation         Bit       7       6       5       4       3         Symbol       die_temperature[7:0]         Reset       0       0       0       0         Access       R       R       R       R         FXOS8700CQ, 6-axis sensor with integrated linear accel       Technical data (Rev. 8 — 25 April 2017) at 52.         10.1.2       I²C read/write operations       Single-byte read         The master (or MCU) transmits a start condition (ST) to t       the slave address, with the R/W bit set to "0" for a write, a acknowledgement. Then the master (or MCU) transmits tread and the FXOS8700CQ sends an acknowledgement a repeated start condition (SR), followed by the slave add for a read from the previously selected register. The FXO and transmits the data from the requested register. The rest of a read from the previously selected register. The rest of the register address read pointer after a read command is following the steps of a single-byte read, multiple bytes o sequential registers after each FXOS8700CQ acknowled acknowledge (NAK) occurs from the master followed by a sequential register after each FXOS8700CQ acknowled acknowledge (NAK) occurs from the master followed by a sequential register after each FXOS8700CQ acknowled acknowledge (NAK) occurs from the master followed by a sequential register after each FXOS8700CQ acknowled acknowledge (NAK) occurs from the master followed b	Temperature data is only valid between -40 °C and 125 °C. The output is only valid when M_CTRL_REG1[m_hms] > 0b00. Pleas temperature sensor is uncalibrated and its output for a given tem one device to the next.         Table 50. TEMP register (address 0x51) bit allocation         Bit       7       6       5       4       3       2         Symbol       die_temperature[7:0]       Reset       0       0       0       0         Reset       0       0       0       0       0       0         Access       R       R       R       R       R         FXOS8700CQ, 6-axis sensor with integrated linear accelerometer       Technical data (Rev. 8 — 25 April 2017) at 52.         10.1.2       I²C read/write operations       Single-byte read         The master (or MCU) transmits a start condition (ST) to the FXOS8 the slave address, with the R/W bit set to "0" for a write, and the FX acknowledgement. Then the master (or MCU) transmits the addres read and the FXOS8700CQ sends an acknowledgement. The mast a repeated start condition (SR), followed by the slave address with for a read from the previously selected register. The FXOS8700CQ and transmits the data from the requested register. The FXOS8700CQ and transmits the data from the requested register. The FXOS8700CQ aut the register address read pointer after a read command is received following the steps of a single-byte read, multiple bytes of data can sequential registers after each FXOS8700CQ acknowledgment (AK acknowledge (NAK) occurs from the master followed by a stop condition to end the t	Temperature data is only valid between -40 °C and 125 °C. The temperature output is only valid when M_CTRL_REG1[m_hms] > 0b00. Please note that it temperature sensor is uncalibrated and its output for a given temperature will one device to the next.         Table 50. TEMP register (address 0x51) bit allocation         Bit       7       6       5       4       3       2       1         Symbol       die_temperature[7:0]       Reset       0       0       0       0       0         Access       R       R       R       R       R       R       R         FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and may Technical data (Rev. 8 — 25 April 2017) at 52.       10.1.2       I²C read/write operations         Single-byte read       The master (or MCU) transmits a start condition (ST) to the FXOS8700CQ, fo the slave address, with the R/W bit set to "0" for a write, and the FXOS8700CQ acknowledgement. Then the master (or MCU) transmits the address of the regreated start condition (SR), followed by the slave address with the R/W bi for a read from the previously selected register. The FXOS8700CQ then ackn and transmits the data from the requested register. The FXOS8700CQ automatically the register address read pointer after a read command is received. Therefore following the steps of a single-byte or "burst" read, the FXOS8700CQ automatically the register address read pointer after a read command is received. Therefore following the steps of a single-byte read, multiple bytes of data can be read from the requester followed by a stop condition (SP) is acknowledge (NAK) occurs from the master	Temperature data is only valid between -40 °C and 125 °C. The temperature sensor output is only valid when M_CTRL_REG1[m_hms] > 0b00. Please note that the temperature sensor is uncalibrated and its output for a given temperature will vary from one device to the next.         Table 50.       TEMP register (address 0x51) bit allocation         Bit       7       6       5       4       3       2       1       0         Symbol       die_temperature[7:0]       memory and the sensor is uncalibrated and its output for a given temperature will vary from one device to the next.         FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer. Technical data (Rev. 8 — 25 April 2017) at 52.         10.1.2       I²C read/write operations         Single-byte read         The master (or MCU) transmits a start condition (ST) to the FXOS8700CQ, followed by the slave address, with the R/W bit set to "0" for a write, and the FXOS8700CQ sends an acknowledgement. Then the master (or MCU) transmits the address of the register to read and the FXOS8700CQ sends an acknowledgement. The master (or MCU) transmits a stare address with the R/W bit set to "1" for a read from the previously selected register. The FXOS8700CQ then acknowledges and transmits the data from the requested register. The FXOS8700CQ automatically increments the register address read pointer after a read command is received. Therefore, after following the steps of a single-byte read, multiple bytes of data can be read from sequential registers after each FXOS8700CQ acknowledgement (AK) is received until a no acknowledge (NAK) occurs from the master followed by a stop condition (SP) signaling an

'474 Patent Claim	Representative NXP Product(s)
	FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer, Data sheet: Technical data (Rev. 8 — 25 April 2017) at 15.
	< Single-byte read >
	Master     ST     Device address[6:0]     W     Register address[7:0]     SR     Device address[6:0]     R     NAK     SP
	Slave AK AK AK Data[7:0]
	< Multiple-byte read >
	Master         ST         Device address[6:0]         W         Register address[7:0]         SR         Device address[6:0]         R         AK
	Slave AK AK AK Data[7:0]
	Master AK AK NAK SP
	Slave         Data[7:0]         Data[7:0]         Data[7:0]
	FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer, Data sheet:         Technical data (Rev. 8 — 25 April 2017) at 16.         10.2.2 SPI read/write operations         A read operation is initiated by transmitting a 0 for the R/W bit. Then the 8-bit register         address, ADDR[7:0] is encoded in the first and second serialized bytes. Subsequent bits
	FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer, Data sheet: Technical data (Rev. 8 — 25 April 2017) at 18.

'474 Patent Claim	'474 Patent Claim Representative NXP Product(s)				
	1 General description				
	The FXPS7115D4 high-performance, high-precision barometric absolute pressure (BAP) sensor consists of a compact capacitive micro-electro-mechanical systems (MEMS) device coupled with a digital integrated circuit (IC) producing a fully calibrated digital output.				
	The sensor is based on NXP's high-precision capacitive pressure cell technology. The architecture benefits from redundant pressure transducers as an expanded quality measure. This sensor delivers highly accurate pressure and temperature readings through either a serial peripheral interface (SPI) or an inter-integrated circuit (I <sup>2</sup> C) interface. The FXPS7115D4 uses either a 3.3 V or 5.0 V power supply. Furthermore, the sensor employs an on-demand digital self-test for the digital IC and the MEMS transducers.				
	FXPS7115D4, Digital absolute pressure sensor, 40 kPa to 115 kPa, Product data sheet (Rev. 4 July 2020) at 1.	<b>4</b> — 17			

474 Patent Claim			Representativ	e NXP Product(s)			
	7.3.4	Temperature senso	r				
	7244	<b>T</b>					
	1.3.4.1	remperature sensor s	signal chain				
		The device includes a t <u>Figure 12</u> shows a simple specified in <u>Table 104</u> a	emperature sensor for signa olified block diagram. Tempe and <u>Table 105</u> .	al compensation and user readabili erature sensor parameters are	ty.		
		temperature sensor CO		VING RAGE AND GAIN TRIM			
		Figure 12. Temperatur	e sensor signal chain block d	liagram	0		
	7.3.4.2	Temperature sensor of	output scaling equation				
		Equation 5 is used to c Table 8.	onvert temperature readings	with the variables specified in			
			$T_{DEGC} = \frac{T_{LSB} - T0_{LS}}{T_{SENSE}}$	<u>u</u>	(5)		
		where:					
		T <sub>DEGC</sub> = The tempe T <sub>LSB</sub> = The tempera	rature output in degrees C ture output in LSB				
	T0 <sub>LSB</sub> = The expected temperature output in LSB at 0 °C						
		T <sub>SENSE</sub> = The expect	ted temperature sensitivity i	n LSB/°C			
		Table 8. Temperature c	onversion variables	11			
		Data reading	TOLSB (LSB)	TBENDE LSB/C)			
	1	8-bit register read	68	1			

7.6       User-accessible         A user-accessible data       of a one time program         programmable block,       incorporate independ         Table 33.       User-accessible data sensor spector         Address       Register         Type <sup>(1)</sup> 7         General device Information       00h         ODh       COUNT         01h       DEVSTAT         R       DBP_ERR	e data array ata array allows each device to be customized. The array consists immable (OTP) factory-programmable block, an OTP user- c, and read-only registers for data and device status. The OTP blocks dent data verification. ecific information Bit 5 4 3 2 1 0 COUNT[7:0]
Table 33. User-accessible data sensor spe       Address     Register     Type <sup>[1]</sup> 7     6       Ceneral device information       00h     COUNT     R       01h     DEVSTAT     R     DSP_ERR	State         State <th< td=""></th<>
Address Register Type <sup>[1]</sup> 7         6           General device Information         00h         COUNT         R           00h         COUNT         R         00h         DDP_ERR         reserver	B# 5 4 3 2 1 0 COUNT[7:0]
General device Information       00h     COUNT       01h     DEVSTAT       R     DSP_ERR	S 5 4 3 2 1 0 COUNT[7:0]
Ceneral device Information           00h         COUNT         R           01h         DEVSTAT         R         DSP_ERR	COUNT[7:0]
01h DEVSTAT R DSP_ERR reserv	COONITION
	Ned COMM ERR MEMTEMP SUPPLY TESTMODE DEVRES DEVINIT
	ERR ERR
02n DEVSTATI R VOCUV_ reserv	Ned VOCOV_ reserved INTREGA_ INTREG_ INTREGF_ CONT_ERR
D3h DEVSTAT2 R F_OTP_ERR U_OT ERR	TP_U_RW_ERR U_W_ reserved TEMP0_ reserved reserved IR ACTIVE R
04h DEVSTAT3 R MISO_ERR OSCTR/	RAIN_ reserved reserved reserved reserved reserved reserved
05h reserved R	reserved
O6h to reserved R ODh	reserved
0Eh TEMPERATURE R	TEMP[7:0]
OFn reserved R	reserved
'474 Patent Claim	Representative NXP Product(s)
-------------------	--
	7.4.6.2 Register read transfers The device supports I <sup>2</sup> C register read data transfers. Register read data transfers are constructed as follows:
	<ol> <li>Constructed as follows:</li> <li>The master transmits a START condition.</li> <li>The master transmits the 7-bit slave address.</li> <li>The master transmits a '0' for the read/write bit to indicate a write operation.</li> <li>The slave transmits an ACK.</li> <li>The master transmits the register address to be read.</li> <li>The slave transmits an ACK.</li> <li>The master transmits a repeat START condition.</li> <li>The master transmits the 7-bit slave address.</li> <li>The master transmits a repeat START condition.</li> <li>The master transmits a '1' for the read/write bit to indicate a read operation.</li> <li>The slave transmits an ACK.</li> <li>The master transmits an ACK.</li> <li>The master transmits an ACK.</li> <li>The master transmits a START condition.</li> </ol>
	SILAVE ADDRESS W A REGISTER ADDRESS A ISTATT SILAVE ADDRESS R A REGISTER DATA N P Master transmission STAVE transmission FXPS7115D4, Digital absolute pressure sensor, 40 kPa to 115 kPa, Product data sheet (Rev. 4 — 17 July 2020) at 16.

'474 Patent Claim		Representative NXP Product(s)
	7.5.3	Command summary
	7.5.3.1	Register read command
		The device supports a register read command. The register read command uses the upper 7 bits of the addresses defined in <u>Section 7.6 "User-accessible data array"</u> to address 8-bit registers in the register map.
		The response to a register read command is shown in <u>Section 7.5.3.1.2 "Register read</u> response message format". The response is transmitted on the next SPI message if and only if all of the following conditions are met:
		<ul> <li>No SPI error is detected (see <u>Section 7.5.5.3 "SPI error"</u>)</li> <li>No MISO error is detected (see <u>Section 7.5.5.4 "SPI data output verification error"</u>)</li> </ul>
		If these conditions are met, the device responds to the register read request as shown in <u>Section 7.5.3.1.2 "Register read response message format"</u> . Otherwise, the device responds with the error response as defined in <u>Section 7.5.5.2 "Detailed status field"</u> . The register read response includes the register contents at the rising edge of SS_B for the register read command.
	FXPS71 July 2020	15D4, Digital absolute pressure sensor, 40 kPa to 115 kPa, Product data sheet (Rev. 4 — 17 0) at 20.

'474 Patent Claim		Representative NXP Product(s)					
	7.5.3.1.1 Registe	r read command message	format				
	Table 13. Register read comma	and message format					
	MSB: bit 31; LSB: bit 0						
	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0						
		Register acces	s command				
	Command Fixed bits: C[3:0] must = 0h	Register address	Register data	8-bit CRC			
	1 1 0 0 0 0 0 0	RA[7:1] RA[0]	0 0 0 0 0 0 0 0	CRC[7:0]			
	Bit field           C[3:0]           RA[7:0]           CRC[7:0]           7.5.3.1.2           Register           Table 15. Register read respon           MSB: bit 31; LSB: bit 0           31         30         29         28         27         26         25         24	Definition           Register           RA[7:1] i           Read CF           er read response message i           ise message format           23         22         21         20         19         18         17         16	n read command = '1100' contains the word address of the register to 1 RC Section format	6 5 4 3 2 1 0			
		Register acces	15 14 13 12 11 10 5 6 7 s command	0 3 4 3 2 1 0			
	Command Basic Unused	Register data: contents	Register data: contents	8-bit CRC			
		RD[15:8]	RDI7:01	CRCI7:01			
	FXPS7115D4, Digital July 2020) at 20.	absolute pressure s	ensor, 40 kPa to 115	kPa, Product data			
	Table 16 Perinter rear	response message hi	t field descriptions				
	Table To. Register reat	a response message si	t held descriptions				
	Bit field	Definition	t neid descriptions				
	Bit field [ C[0], [3:1] F	Definition Register Read Command = '01'					
	Bit field         I           C[0], [3:1]         I           ST[1:0]         ST	Definition Register Read Command = '01' Status	10'				
	Bit field         I           C[0], [3:1]         I           ST[1:0]         ST[1:8]	Definition Register Read Command = '01' Status The contents of the register add	10' Iressed by RA[7:1] high byte (RA[0]	= 1)			
	Bit field         I           C[0], [3:1]         I           ST[1:0]         S           RD[15:8]         T           RD[7:0]         T	Definition Register Read Command = '01' Status The contents of the register add The contents of the register add	10' Iressed by RA[7:1] high byte (RA[0] Iressed by RA[7:1] low byte (RA[0] =	= 1) = 0)			

'474 Patent Claim	Representative NXP Product(s)				
[8c.] in response to the read temperature command, the serial interface slave supplying over the data signal line a temperature value associated with a processor on an integrated circuit containing the serial	The Accused '474 Sensors performs a step of in response to the read temperature command, the serial interface slave supplying over the data signal line a temperature value associated with a processor on an integrated circuit containing the serial interface slave. For example, each of the Accused '474 Sensors perform a step of in response to the read temperature command, the serial interface slave identified above supplying over the data signal line identified above a temperature value ( <i>e.g.</i> , the temperature value in the TEMP_OUT register) associated with a processor on an integrated circuit containing the serial interface slave identified above.				
interface slave.	<ul> <li>2 Features and benefits         <ul> <li>±2/4/8/16 g user-selectable, full-scale measurement ranges</li> <li>12-bit acceleration data</li> <li>8-bit temperature sensor data</li> <li>Low noise: 280 µg/\Hz in high performance mode</li> <li>Low power capability:                 <ul> <li>≤ 1 µA I<sub>DD</sub> for ODRs up to 6.25 Hz</li> <li>&lt; 4 µA I<sub>DD</sub> for ODRs up to 50 Hz</li> </ul> </li> </ul> </li> <li>FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 1.</li> </ul>				



'474 Patent Claim	Representative NXP Product(s)			
	10 I <sup>2</sup> C digital interface			
	The registers embedded within FXLS8962AF may be accessed using an $I^2C$ interface when the INTF_SEL pin is tied to GND. If the V <sub>DD</sub> supply is not present, the device will be in shutdown mode and any communications on the interface are ignored. When the device is on a common $I^2C$ -bus with other slave devices, the V <sub>DD</sub> supply pin must be left unconnected (high-impedance) when the device supply is turned off to ensure that the internal ESD protection diodes do not become forward biased and prevent the bus from functioning normally (clamping).			
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 16.			
	10.1.2 I <sup>2</sup> C read/write operations			
	10.1.2.1 Single byte read			
	The master transmits a start condition (ST) to FXLS8962AF, followed by the slave address, with the R/W bit set to '0' for a write, and the FXLS8962AF sends an acknowledgement. Then the master transmits the address of the register to read and the FXLS8962AF sends an acknowledgement. The master transmits a repeated start condition (SR), followed by the slave address with the R/W bit set to '1' for a read from the previously selected register. The FXLS8962AF then acknowledges and transmits the data from the requested register. The master does not acknowledge (NAK) the transmitted data and then transmits a stop condition to end the data transfer.			
	10.1.2.2 Multiple byte read			
	When performing a multi-byte or <i>burst</i> read, FXLS8962AF automatically increments the register read address pointer after a read command is received. Therefore, after following			
	the steps of a single-byte read, multiple bytes of data can be read from sequential register addresses after each FXLS8962AF acknowledgment (ACK) is received until a no acknowledge (NAK) is issued by the master followed by a stop condition (SP) signaling the end of the transfer.			
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18- 19.			



'474 Patent Claim	Representative NXP Product(s)
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18- 20-21.
	11.3 SPI read operations with 4-wire mode A register read operation is initiated by transmitting a 1 for the R/W bit. Then, the 7- bit register read address, A[6:0] is encoded in the first byte. Following this first byte, a second byte of 0s or 1s (don't care condition) is transferred. After this transfer completes, the next 8 SCLK cycles (pulses 17 through 24) output the selected register content on the SPI MISO line in MSb first order. The following figure shows the bus protocol for a single byte read operation.
	$SPI_{CS_B} $ $SCLK \_ 1 \sqrt{2} \sqrt{3} \sqrt{4} \sqrt{5} \sqrt{6} \sqrt{7} \sqrt{8} \sqrt{9} \sqrt{10} \sqrt{11} \sqrt{12} \sqrt{13} \sqrt{14} \sqrt{15} \sqrt{16} \sqrt{17} \sqrt{18} \sqrt{19} \sqrt{20} \sqrt{21} \sqrt{22} \sqrt{23} \sqrt{24} $ $SPI_{MOSI} \_ \overline{RW} \sqrt{A6} \sqrt{A5} \sqrt{A4} \sqrt{A3} \sqrt{A2} \sqrt{A1} \sqrt{A0} \sqrt{X} \sqrt{X} \sqrt{X} \sqrt{X} \sqrt{X} \sqrt{X} \sqrt{X} X$
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18- 21-22.

'474 Patent Claim	Representative NXP Product(s)
	Multiple-byte read operations are performed similarly to single-byte reads with additional bytes read out in multiples of eight SCLK cycles. The register read address is auto- incremented by FXLS8962AF so that every eighth clock edge will latch the address of the next sequential register read address. When the desired number of bytes has been read, a rising edge on SPI_CS_B terminates the transaction.
	SPLCS_B
	SCLK1 2 3 4 5 6 7 7 6 1 6 1 7 1 2 1 3 1 4 1 5 1 6 1 7 1 8 1 6 20 2 1 2 2 2 2 2 4 2 6 2 7 2 9 2 9 2 9 3 1 5 2
	$spl_Mosi = - RW(Ab(Ab(Ab(Ab(Ab(Ab(X)(Ab(X)(X$
	SPI_MISO
	Figure 15. SPI multiple byte read protocol diagram (4-wire mode), R/W = 1
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18- 22.
	11.4 SPI read operations with 3-wire mode FXLS8962AF can be configured to operate in 3-wire software enabled SPI mode. In this mode, the SPI MISO pin is left unconnected and the SPI MOSI pin becomes a bidimeticated introduction (SPI DATA). Deed competition in 2-wire mode and the
	bidirectional input/output pin (SPI_DATA). Read operations in 3-wire mode are the same as write operations in 3- and 4-wire modes, except that at the end of the address cycle (falling edge of clock pulse 16), the SPI_DATA pin automatically switches from an input to an output and with bit D7 as the current output state.
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18- 22.

'474 Patent Claim	Representative NXP Product(s)
	$[SPL_GS_B] = [SCLK \_ (\sqrt{2}\sqrt{3}\sqrt{4}\sqrt{5}\sqrt{6}\sqrt{7}\sqrt{8}\sqrt{9}\sqrt{6}\sqrt{1}\sqrt{12}\sqrt{13}\sqrt{4}\sqrt{15}\sqrt{16}\sqrt{19}\sqrt{19}\sqrt{19}\sqrt{20}\sqrt{21}\sqrt{22}\sqrt{21}\sqrt{24}\sqrt{24}\sqrt{24}\sqrt{24}\sqrt{24}\sqrt{24}\sqrt{24}24$

'474 Patent Claim	Representative NXP Product(s)									
	14.3 Temperature register									
	14.3.1 TEMP register (address 0x51)									
	Eight-bit 2's complement sensor temperature value with 0.96 °C/LSB sensitivity.									
		1	Temperature o	perature data is only valid between -40 °C and 125 °C. The temperature sensor				esensor		
	output is only valid when M_CTRL_REG1[m_hms] > 0b00. Please note that the temperature sensor is uncalibrated and its output for a given temperature will vary from									
			one device to	the next.					Construction of the	
	Table 50.	TEMP regist	er (address 0x	51) bit alloca	tion					
	Bit	7	6	5	4	3	2		0	
	Symbol				die_tempe	erature[7:0]				
	Reset	0	0	0	0	0	0	0	0	
	Access	R	ĸ	R	ĸ	ĸ	к	ĸ	R	
	10.1.2 I <sup>2</sup> s	C read/w ingle-byte	rite opera read (or MCU) tr	tions ansmits a s	start condit	ion (ST) to t	the FXOS	3700CQ, fo	llowed by	
	tr	e slave ac	ement The	the R/W bi	er (or MCII	for a write,	and the F)	COS8/00C	Q sends an	
	re	ad and th	FXOS870	OCQ sends	an acknov	vledgement	. The mas	ter (or MCI	J) transmits	
	a	repeated :	start conditio	on (SR), fo	llowed by t	he slave ad	dress with	the R/W b	it set to "1"	
	fo	or a read fr	om the prev	iously sele	cted regist	er. The FXC	S8700CQ	then ackn	owledges	
	a	nd transmi	ts the data f	rom the re	quested re	gister. The r	master doe	es not ackn	owledge	
	(NAK) the transmitted data, but transmits a stop condition to end the data transfer.									
	V	/hen perfo	rming a mult	ti-byte or "b	ourst" read,	the FXOS8	700CQ au	tomatically	increments	
	the register address read pointer after a read command is received. Therefore, after following the steps of a single-byte read, multiple bytes of data can be read from									
	S	equential r	egisters afte	er each FX	DS8700CQ	acknowled	gment (Ak	() is receive	ed until a no	
	a	cknowledg	e (NAK) occ	curs from th	ne master fo	ollowed by a	a stop conc	lition (SP)	signaling an	
	e	na or trans	mission.							
										J

'474 Patent Claim	Representative NXP Product(s)						
	FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer, Data sheet: Technical data (Rev. 8 — 25 April 2017) at 15.						
	< Single-byte read >         Master       ST       Device address[6:0]       W       Register address[7:0]       SR       Device address[6:0]       R       NAK       SP						
	Slave AK AK AK Data[7:0]						
	< Multiple-byte read >           Master         ST         Device address[6:0]         W         Register address[7:0]         SR         Device address[6:0]         R         AK						
	Slave AK AK Data[7:0]						
	Master AK AK NAK SP						
	Slave         Data[7:0]         Data[7:0]         Data[7:0]						
	FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer, Data sheet: Technical data (Rev. 8 — 25 April 2017) at 16.						
	10.2.2 SPI read/write operations						
	A read operation is initiated by transmitting a 0 for the R/W bit. Then the 8-bit register address, ADDR[7:0] is encoded in the first and second serialized bytes. Subsequent bits are ignored by the part. The read data is describilized from the MISO pin						
	are ignored by the part. The read data is desenalized from the MISO pin.						
	FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer, Data sheet: Technical data (Rev. 8 — 25 April 2017) at 18.						

[	'474 Patent Claim	Representative NXP Product(s)					
		1 General description					
		The FXPS7115D4 high-performance, high-precision barometric absolute pressure (BAP) sensor consists of a compact capacitive micro-electro-mechanical systems (MEMS) device coupled with a digital integrated circuit (IC) producing a fully calibrated digital output.					
		The sensor is based on NXP's high-precision capacitive pressure cell technology. The architecture benefits from redundant pressure transducers as an expanded quality measure. This sensor delivers highly accurate pressure and temperature readings through either a serial peripheral interface (SPI) or an inter-integrated circuit (I <sup>2</sup> C) interface. The FXPS7115D4 uses either a 3.3 V or 5.0 V power supply. Furthermore, the sensor employs an on-demand digital self-test for the digital IC and the MEMS transducers.					
		FXPS7115D4, Digital absolute pressure sensor, 40 kPa to 115 kPa, Product data sheet (Rev. 4 – July 2020) at 1.	— 17				

'474 Patent Claim	Representative NXP Product(s)					
	7.3.4	Temperature sens	or			
	100000					
	1.3.4.1	Temperature sensor	r signal chain			
		The device includes a Figure 12 shows a sin specified in <u>Table 104</u>	a temperature sensor for si nplified block diagram. Ter <u>4</u> and <u>Table 105</u> .	gnal compensation and user rea nperature sensor parameters are	idability. e	
		temperature sensor C		MOVING AVERAGE OFFSET AND GAIN TRIM	e output	
		Figure 12. Temperate	ure sensor signal chain bloo	k diagram		
	7.3.4.2	Temperature sensor	r output scaling equation			
		Equation 5 is used to Table 8.	convert temperature readi	ngs with the variables specified i	in	
			$T_{DEGC} = \frac{T_{LSB} - T_{C}}{T_{SENS}}$	V <sub>LSB</sub>	(5)	
		where:				
		T <sub>DEGC</sub> = The temp T <sub>LSB</sub> = The tempe	erature output in degrees rature output in LSB	<u>c</u>		
		TO <sub>LSB</sub> = The expe	cted temperature output in	LSB at 0 °C		
		ISENSE - THE EXP	ected temperature sensitiv	ty in LSbr C		
		Table 8. Temperature	conversion variables	T I BRIOL		
		8-bit register read	68	1		
		1999-999-9999-9999-99 71	12200			
	FXPS711 July 2020	5D4, Digital abso )) at 12.	olute pressure sensor,	40 kPa to 115 kPa, Prod	uct data sheet (Rev. 4 — 17	

7.6 User-accessible data array         A user-accessible data array allows each device to be customized. The array consists of a one time programmable block, and CTP user-programmable block, and read-only registers for data and device status. The OTP blocks incorporate independent data verification.         Table 33. User-accessible data sensor specific information         Address Register       Type <sup>III</sup> Bit         Ceneral device information         Address Register       Type <sup>III</sup> Bit         Convrt_17:0)         ODH       COUNTIT: R			ct(s)	Produc	e NXP	entative	leprese	F				
Table 33. User-accessible data — sensor specific information         Address Register       Type <sup>(1)</sup> Bit         Control State       State         Type <sup>(1)</sup> Bit         Control State       State         Control State       State         Oth       COUNT       R       SUPPLY       TESTMODE       DEVRES       DEVINIT         Oth       COUNT       R       COUNT[7:0]         Oth       DEVSTAT       R       DSP_ERR       COUNT[7:0]         Oth       DEVSTAT       R       DSP_ERR       COUNT[7:0]         OTH       DEVSTAT1       R       DSP_ERR       SUPPLY       TESTMODE       DEVRES       DEVINIT         OTH       DEVSTAT1       R       COCOUNT       ERR       ERR       ERR       ERR       ERR       CONT_ERR         02h <th></th> <td>onsists TP blocks</td> <td>he array c OTP user- tus. The O</td> <td>stomized. T block, an ( device stat</td> <td>e to be cus grammable r data and</td> <td>each devic actory-prog registers fo ation.</td> <td>a array ray allows ble (OTP) f read-only lata verific</td> <td>ble data ar rogramma block, and ependent of</td> <td>er-accessi ser-accessi one time p grammable prporate ind</td> <td>Us A u of a pro</td> <td>7.6</td> <td></td>		onsists TP blocks	he array c OTP user- tus. The O	stomized. T block, an ( device stat	e to be cus grammable r data and	each devic actory-prog registers fo ation.	a array ray allows ble (OTP) f read-only lata verific	ble data ar rogramma block, and ependent of	er-accessi ser-accessi one time p grammable prporate ind	Us A u of a pro	7.6	
Address     Register     Type <sup>ITI</sup> Bit       7     6     5     4     3     2     1     0       General device information     COUNT     R     COUNT[7:0]     COUNT[7:0]       01h     DEVSTAT     R     DSP_ERR     reserved     COMM_ERR     MEMTEMP_ ERR     SUPPLY_ ERR     TESTMODE     DEVRES     DEVINIT       02h     DEVSTAT1     R     VCCUV_ ERR     reserved     COMM_ERR     MEMTEMP_ ERR     SUPPLY_ ERR     TESTMODE     DEVRES     DEVINIT       03h     DEVSTAT2     R     F_OTP_ERR     U_OTP_ ERR     U_W_ ERR     reserved     TEMP0_ ERR     reserved     reserved							informatio	or specific	data - sens	sible	3. User-acces	Table 3
7     6     5     4     3     2     1     0       General device information       00h     COUNT     R     COUNT[7:0]       01h     DEVSTAT     R     DSP_ERR     reserved     COMM_ERR     MEMTEMP_ ERR     SUPPLY_     TESTMODE     DEVRES     DEVINIT       02h     DEVSTAT1     R     VCCUV_ ERR     reserved     VCCOV_ ERR     reserved     INTREGA_ ERR     INTREGA_ ERR     INTREGA_ ERR     INTREGF_ ERR     CONT_ERR       03h     DEVSTAT2     R     F_OTP_ERR     U_OTP_ FERR     U_W_ ACTIVE     reserved     reserved     reserved     reserved					t:	BI			tul.	Туре	Register	Address
Ceneral device information       00h     COUNT     R     COUNT[7:0]       01h     DEVSTAT     R     DSP_ERR     reserved     COMM_ERR     MEMTEMP_ ERR     SUPPLY_ ERR     TESTMODE     DEVRES     DEVINIT       02h     DEVSTAT1     R     VCCUV_ ERR     reserved     VCCOV_ ERR     reserved     INTREGA_ ERR     INTREGA_ ERR     INTREGF_ ERR     CONT_ERR       03h     DEVSTAT2     R     F_OTP_ERR     U_OTP_ ERR     U_W_ ERR     reserved     reserved ERR     reserved ERR     reserved     reserved		0	1	2	3	4	5	6	7			
Oth     DEVSTAT     R     DSP_ERR     reserved     COMM_ERR     METTEMP_ ERR     DSPLPLY_ ERR     TESTMODE     DEVRES     DEVINIT       02h     DEVSTAT1     R     VCCUV_ ERR     reserved     VCCOV_ ERR     reserved     INTREGA_ ERR     INTREGA_ ERR     INTREGF_ ERR     CONT_ERR       03h     DEVSTAT2     R     F_OTP_ERR     U_OTP_ ERR     U_W_ ERR     reserved     TEMP0_ ERR     reserved     reserved										1	device Information	General
02h     DEVSTATI     R     VOCUV_ ERR     reserved     VOCOV_ ERR     reserved     INTREGA_ ERR     INTREGA_ ERR     INTREGF_ ERR     CONT_ERR       03h     DEVSTAT2     R     F_OTP_ERR     U_OTP_ ERR     U_W_ ERR     reserved     TEMPO_ ERR     reserved     reserved		DEVINIT	DEVRES	TESTMODE	SUPPLY	MEMTEMP	COMM ERR	reserved	DSP ERR	R	DEVSTAT	00h
02h     DEVSTATI     R     VCCUV_ ERR     reserved     VCCOV_ ERR     reserved     INTREG_ ERR     INTREG_ ERR     INTREG_ ERR     INTREG_ ERR     INTREG_ ERR     CONT_ERR       03h     DEVSTAT2     R     F_OTP_ERR     U_ORW_ERR     U_W ERR     reserved     TEMP0_ ERR     reserved     reserved					ERR	ERR				10°		-
03h DEVSTAT2 R F_OTP_ERR U_OTP_ U_RW_ERR U_W reserved TEMP0_ reserved reserved reserved		CONT_ERR	INTREGF_	INTREG_ ERR	INTREGA_	reserved	VCCOV_	reserved	VCCUV_ ERR	R	DEVSTAT1	02h
LIN NOIVE EN		reserved	reserved	TEMP0_ ERR	reserved	U_W_ ACTIVE	U_RW_ERR	U_OTP_ ERR	F_OTP_ERR	R	DEVSTAT2	03h
04h DEVSTAT3 R MISO_ERR OSCTRAIN_ reserved reserved reserved reserved reserved reserved reserved reserved reserved		reserved	reserved	reserved	reserved	reserved	reserved	OSCTRAIN_ ERR	MISO_ERR	R	DEVSTAT3	04h
OSh reserved R reserved					ved	reser		2		R	reserved	05h
OBh to reserved R reserved ODh					ved	reser				R	reserved	O6h to ODh
DEh TEMPERATURE R TEMP[7:0]					[7:0]	TEMP				R	TEMPERATURE	OEh
OFn reserved R reserved					ved	reser			1	R	reserved	OFn

	Representative NXP Product(s)
	Representative NXP Product(s)         7.4.6.2 Register read transfers         The device supports I <sup>2</sup> C register read data transfers. Register read data transfers are constructed as follows:         1. The master transmits a START condition.       2. The master transmits the 7-bit slave address.         3. The master transmits a '0' for the read/write bit to indicate a write operation.       4. The slave transmits an ACK.         5. The master transmits the register address to be read.       6. The slave transmits an ACK.         7. The master transmits a repeat START condition.       8. The master transmits the 7-bit slave address.         9. The master transmits the 7-bit slave address.       9. The master transmits a '1' for the read/write bit to indicate a read operation.
F	<ul> <li>8. The master transmits the 7-bit slave address.</li> <li>9. The master transmits a '1' for the read/write bit to indicate a read operation.</li> <li>10. The slave transmits an ACK.</li> <li>11. The slave transmits the data from the register addressed.</li> <li>12. The master transmits a NACK.</li> <li>13. The master transmits a STOP condition.</li> </ul>

'474 Patent Claim		Representative NXP Product(s)
	7.5.3	Command summary
	7.5.3.1	Register read command
		The device supports a register read command. The register read command uses the upper 7 bits of the addresses defined in <u>Section 7.6 "User-accessible data array"</u> to address 8-bit registers in the register map.
		The response to a register read command is shown in <u>Section 7.5.3.1.2 "Register read</u> <u>response message format"</u> . The response is transmitted on the next SPI message if and only if all of the following conditions are met:
		<ul> <li>No SPI error is detected (see Section 7.5.5.3 "SPI error")</li> <li>No MISO error is detected (see Section 7.5.5.4 "SPI data output verification error")</li> </ul>
		If these conditions are met, the device responds to the register read request as shown in <u>Section 7.5.3.1.2 "Register read response message format"</u> . Otherwise, the device responds with the error response as defined in <u>Section 7.5.5.2 "Detailed status field"</u> . The register read response includes the register contents at the rising edge of SS_B for the register read command.
	FXPS71 July 202	15D4, Digital absolute pressure sensor, 40 kPa to 115 kPa, Product data sheet (Rev. 4 — 17 0) at 20.

'474 Patent Claim		Rep	presentative NXP Pro	duct(s)	
	7.5.3.1.1 Regis	ster read command messag	ge format		]
	Table 13. Register read com	mand message format			
	MSB: bit 31; LSB: bit 0				
	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	i 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
		Register ac	cess command		
	Command Fixed bits: C[3:0] must = 0h	Register address	Register data	8-bit CRC	
	1 1 0 0 0 0 0 0	RA[7:1] RA[	0 0 0 0 0 0 0 0 0	CRC[7:0]	
	Table	14 Persister read comman	d message hit field descriptions		
	Bit fiel	ld Defin	ition		
	C[3:0]	Regis	ster read command = '1100'		
	RA[7:0	] RA[7:	1] contains the word address of the register	to be read.	
	CRC[7	:0] Read	CRC Section		
	7.5.3.1.2 Regis	ster read response messag	e format		
	Table 45 Desister read room				
	MSB: bit 31: LSB: bit 0	onse message format			
	31 30 29 28 27 26 25	24 23 22 21 20 19 18 17	16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
		Register ac	cess command		
	Command Basic Unus C[0], [3:1] Status Data	ed Register data: contents 0h of RA[7:1] high byte	Register data: contents of RA[7:1] low byte	8-bit CRC	
	0 1 1 0 ST[1:0] 0	0 RD[15:8]	RD[7:0]	CRC[7:0]	
	FXPS7115D4, Digita July 2020) at 20.	ll absolute pressure	sensor, 40 kPa to 11	5 kPa, Product data	」 sheet (Rev. 4 — 17
			and the second		7
	Table 16. Register re	ad response message	bit field descriptions		
	Bit field	Definition			
	C[0], [3:1]	Register Read Command = '(	0110'		
	ST[1:0]	Status			
	RD[15:8]	The contents of the register a	iddressed by RA[7:1] high byte (RA	[0] = 1)	
	RD[7:0]	The contents of the register a	ddressed by RA[7:1] low byte (RA[0	0] = 0)	
	CRC[7:0]	8-bit CRC			
	EXPS7115D/ Digita	l absolute pressure	sensor 10 kPa to 11	5 kPa Product data	sheet (Rev. 1
	$1^{-1}X_{1}S/115D_{-1}$ , Digita	ii absolute pressure	5011501, 40 KI a 10 11.		sheet (ICev. $4 - 1$ )
	July 2020) at 21.				

'474 Patent Claim	Representative NXP Product(s)
[14a.] A serial communication system comprising:	To the extent the preamble is limiting, the Accused '474 Sensors include a "serial communication system" as recited in the '474 patent. Exemplary systems and serial interfaces are identified in the block diagrams and rectangles below.
	See, e.g.:
	https://www.avnet.com/shop/us/products/nxp/fxos8700cqr1- 3074457345626313537?fromPage=autoSuggest&langId=-1&autoSuggestSearchTerm=FXOS

















'474 Patent Claim	Representative NXP Product(s)
	10.1.2 I <sup>2</sup> C read/write operations
	The master transmits a start condition (ST) to FXLS8962AF, followed by the slave address, with the R/W bit set to '0' for a write, and the FXLS8962AF sends an acknowledgement. Then the master transmits the address of the register to read and the FXLS8962AF sends an acknowledgement. The master transmits a repeated start condition (SR), followed by the slave address with the R/W bit set to '1' for a read from the previously selected register. The FXLS8962AF then acknowledges and transmits the data from the requested register. The master does not acknowledge (NAK) the transmitted data and then transmits a stop condition to end the data transfer.
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18.
	The SPI interface is a classical Master/Slave serial port. FXLS8962AF is always considered to be the slave device and thus never initiates communication with the host processor.
	The SPI interface of FXLS8962AF is compatible with interface mode 00, corresponding to CPOL = 0 and CPHA = 0.
	For CPOL = 0, the idle value of the clock is zero, and the active value of the clock is 1. For CPHA = 0, data is captured on the clock's rising edge (low to high transition) and data is propagated on the clock's falling edge (high to low transition).
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 20.
	10.1.1 General I <sup>2</sup> C operation There are two signals associated with the I <sup>2</sup> C-bus: the Serial Clock Line (SCL) and the Serial Data line (SDA). SDA is a bidirectional signal used for sending and receiving the data to/from the interface. External pull-up resistors connected to V <sub>DD</sub> are required for SDA and SCL. When the I <sup>2</sup> C-bus is free, SCL and SDA are high.

'474 Patent Claim	Representative NXP Product(s)
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18.
	<b>11.1</b> General SPI operation         The SPI_CS_B pin is driven low at the start of a transaction, held low for the duration of the transfer, and then driven high again after the transaction is completed. During a transaction, the master toggles the clock (SCLK). The SCLK polarity is defined as having an idle value that is low, and an active phase that is high (CPOL = 0). Serial input and output data is captured on the clock's rising edge and propagated on the falling edge         FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 20.
	11.4       SPI read operations with 3-wire mode         FXLS8962AF can be configured to operate in 3-wire software enabled SPI mode. In         this mode, the SPI_MISO pin is left unconnected and the SPI_MOSI pin becomes a         bidirectional input/output pin (SPI_DATA). Read operations in 3-wire mode are the same         as write operations in 3- and 4-wire modes, except that at the end of the address cycle         (falling edge of clock pulse 16), the SPI_DATA pin automatically switches from an input         to an output and with bit D7 as the current output state.         FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 22.

'474 Patent Claim	Representative NXP Product(s)				
	SDA / SPI_MOSI / SPI_DATA	4	<ul> <li>Mode dependent Multifunction serial interface pin.<sup>[2]</sup></li> <li>INTF_SEL = V<sub>DD</sub>:</li> <li>SPI_MOSI: In 4-wire SPI mode this pin functions as the serial data input (Master Out Slave In).</li> <li>SPI_DATA<sup>[3]</sup>. In 3-wire SPI mode this pin functions as the bidirectional serial data input/output.</li> <li>INTF_SEL = GND:</li> <li>SDA: This pin functions as the I<sup>2</sup>C Serial Data input/output.</li> </ul>		
	SCL / SCLK	5	Mode dependent Multifunction serial interface pin. <sup>[2]</sup> INTF_SEL = V <sub>DD</sub> : • SPI serial clock input (3- and 4-wire modes) INTF_SEL = GND: • I <sup>2</sup> C serial clock input		
	FXLS8962AF, 3-Axis Lov	w-g Ac	ccelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 4.		



'474 Patent Claim	Representative NXP Product(s)
	10.1.2 I <sup>2</sup> C read/write operations Single-byte read
	The master (or MCU) transmits a start condition (ST) to the FXOS8700CQ, followed by the slave address, with the R/W bit set to "0" for a write, and the FXOS8700CQ sends an acknowledgement. Then the master (or MCU) transmits the address of the register to read and the FXOS8700CQ sends an acknowledgement. The master (or MCU) transmits a repeated start condition (SR), followed by the slave address with the R/W bit set to "1" for a read from the previously selected register. The FXOS8700CQ then acknowledges and transmits the data from the requested register. The master does not acknowledge (NAK) the transmitted data, but transmits a stop condition to end the data transfer.
	FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer, Data sheet: Technical data (Rev. 8 — 25 April 2017) at 15.
	There are two signals associated with the I <sup>2</sup> C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. External pullup resistors connected to VDDIO are required for SDA and SCL. When the bus is free both the lines are high. The I <sup>2</sup> C interface is compliant with fast mode (400 kHz), and normal mode (100 kHz) I <sup>2</sup> C standards. Operation at frequencies higher than 400 kHz is possible, but depends on several factors including the pullup resistor values, and total bus capacitance (trace + device capacitance). See <u>Table 11</u> for more information.
	FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer, Data sheet: Technical data (Rev. 8 — 25 April 2017) at 14.

	Representative NXP Product(s)	
10.2.1 Gen	eral SPI operation	
TOLET OCH	NOTE	
	NUTE	
	one master (MCU) and one slave device (FXOS8700CQ) present on the bus. FXOS8700CQ does not tri-state the MISO pin when the CS_B pin is deasserted (logic high), which can lead to a bus conflict if multiple slave devices are present on the bus.	
	Do not connect more than one master and one slave device on the SPI bus.	
trans mast	CS_B pin is driven low at the start of a SPI transaction, held low for the duration of the action, and driven high after the transaction is complete. During a transaction the ter toggles the SPI clock (SCLK) and transmits data on the MOSI pin.	e
FXOS8700C Technical dat	Q, 6-axis sensor with integrated linear accelerometer and magnetometer a (Rev. 8 — 25 April 2017) at 17.	er, Data sheet:
FXOS8700C0 Technical dat	Q, 6-axis sensor with integrated linear accelerometer and magnetometer a (Rev. 8 — 25 April 2017) at 17.	 er, Data sheet:
FXOS8700C0 Technical dat	Q, 6-axis sensor with integrated linear accelerometer and magnetometer ca (Rev. 8 — 25 April 2017) at 17.	 er, Data sheet:
FXOS8700C0 Technical dat	Q, 6-axis sensor with integrated linear accelerometer and magnetometer a (Rev. 8 — 25 April 2017) at 17. ial interface pin descriptions Pin description Digital interface power	 er, Data sheet:
FXOS8700C0 Technical dat	Q, 6-axis sensor with integrated linear accelerometer and magnetometer a (Rev. 8 — 25 April 2017) at 17. ial interface pin descriptions Pin description Digital interface power I <sup>2</sup> C second least significant bit of device address/SPI chip select	er, Data sheet:
FXOS8700C0 Technical dat Table 13. Ser Pin name VDDIO SA1/CS_B SCL/SCLK	Q, 6-axis sensor with integrated linear accelerometer and magnetometer ra (Rev. 8 — 25 April 2017) at 17.	er, Data sheet:
FXOS8700C0 Technical dat	Q, 6-axis sensor with integrated linear accelerometer and magnetometer ia (Rev. 8 — 25 April 2017) at 17. ial interface pin descriptions Pin description Digital interface power I <sup>2</sup> C second least significant bit of device address/SPI chip select I <sup>2</sup> C/SPI serial clock I <sup>2</sup> C serial data/SPI master serial data out slave serial data in	



'474 Patent Claim			Representative NXP Product(s)			
	7.4.1 I <sup>2</sup> C b The s must After Timin	it transmission tate of SDA wher be stable when S the START signa g for the start con	n SCL is high determines the bit value being transmitted. SDA CL is high and change when SCL is low as shown in <u>Figure 14</u> . I has been transmitted by the master, the bus is considered busy. Indition is specified in <u>Table 105</u> .			
	FXPS7115D4, Digital absolute pressure sensor, 40 kPa to 115 kPa, Product data sheet (Rev. 4 July 2020) at 13.					
	7.5       Standard 32-bit SPI protocol         The device includes a standard SPI protocol requiring 32-bit data packets. The device is a slave device and requires that the base clock value be low (CPOL = 0) with data captured on the rising edge of the clock and data propagated on the falling edge of the clock (CPHA = 0). The most significant bit is transferred first (MSB first). SPI transfers are completed through a sequence of two phases. During the first phase, the command is transmitted from the SPI master to the device. During the second phase, response data is transmitted from the slave device. MOSI and SCLK transitions are ignored when SS_B is not asserted.         FXPS7115D4, Digital absolute pressure sensor, 40 kPa to 115 kPa, Product data sheet (Re July 2020) at 17.         9       SCLK/SCL       In I <sup>2</sup> C mode, input pin 9 provides the serial clock. This pin must be connected to V <sub>cc</sub> with an external pull-up resistor, as shown in the application diagram. In SPI mode, input pin 9 provides the serial clock. An internal pull-down device is					
	10     MOSI     SPI data in In SPI mode, pin 10 functions as the serial data input to the SPI port. An internal pull-down device is connected to this pin.					
	FXPS7115D July 2020) at	4, Digital abso 4.	lute pressure sensor, 40 kPa to 115 kPa, Product data sheet (Rev. 4 — 17			
[14d.] wherein the slave serial interface is	In each of the	e Accused '474	Sensors, the slave serial interface is responsive to a read temperature			

'474 Patent Claim	Representative NXP Product(s)
responsive to a read temperature command issued by the master serial interface to return to the	command issued by the master serial interface to return to the master serial interface a temperature value associated with the microprocessor.
interface to return to the master serial interface a temperature value associated with the microprocessor.	above) is responsive to a read temperature command ( <i>e.g.</i> , the read temperature command directed to the TEMP_OUT register) issued by the master serial interface ( <i>e.g.</i> , the SPI/I2C interface on the master/MCU and/or the host processor identified above) to return to the master serial interface a temperature value ( <i>e.g.</i> , the temperature value in the TEMP_OUT register) associated with the microprocessor identified above.
	<ul> <li>2 Features and benefits         <ul> <li>±2/4/8/16 g user-selectable, full-scale measurement ranges</li> <li>12-bit acceleration data</li> <li>8-bit temperature sensor data</li> <li>Low noise: 280 µg/√Hz in high performance mode</li> <li>Low power capability:</li> <li>≤ 1 µA I<sub>DD</sub> for ODRs up to 6.25 Hz</li> <li>&lt; 4 µA I<sub>DD</sub> for ODRs up to 50 Hz</li> </ul> </li> <li>FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 1.</li> </ul>


'474 Patent Claim	Representative NXP Product(s)
	10 I <sup>2</sup> C digital interface
	The registers embedded within FXLS8962AF may be accessed using an $I^2C$ interface when the INTF_SEL pin is tied to GND. If the V <sub>DD</sub> supply is not present, the device will be in shutdown mode and any communications on the interface are ignored. When the device is on a common $I^2C$ -bus with other slave devices, the V <sub>DD</sub> supply pin must be left unconnected (high-impedance) when the device supply is turned off to ensure that the internal ESD protection diodes do not become forward biased and prevent the bus from functioning normally (clamping).
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 16.
	10.1.2 I <sup>2</sup> C read/write operations
	10.1.2.1 Single byte read The master transmits a start condition (ST) to FXLS8962AF, followed by the slave address, with the R/W bit set to '0' for a write, and the FXLS8962AF sends an acknowledgement. Then the master transmits the address of the register to read and the FXLS8962AF sends an acknowledgement. The master transmits a repeated start condition (SR), followed by the slave address with the R/W bit set to '1' for a read from the previously selected register. The FXLS8962AF then acknowledges and transmits the data from the requested register. The master does not acknowledge (NAK) the transmitted data and then transmits a stop condition to end the data transfer.
	10.1.2.2 Multiple byte read When performing a multi-byte or <i>burst</i> read, FXLS8962AF automatically increments the register read address pointer after a read command is received. Therefore, after following the steps of a single-byte read, multiple bytes of data can be read from sequential register addresses after each FXLS8962AF acknowledgment (ACK) is received until a no
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18- 19.



'474 Patent Claim	Representative NXP Product(s)
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18- 20-21.
	11.3 SPI read operations with 4-wire mode A register read operation is initiated by transmitting a 1 for the R/W bit. Then, the 7- bit register read address, A[6:0] is encoded in the first byte. Following this first byte, a second byte of 0s or 1s (don't care condition) is transferred. After this transfer completes, the next 8 SCLK cycles (pulses 17 through 24) output the selected register content on the SPI MISO line in MSb first order. The following figure shows the bus protocol for a single byte read operation.
	$SPI_{CS_B} $ $SCLK \_ 1 \sqrt{2} \sqrt{3} \sqrt{4} \sqrt{5} \sqrt{6} \sqrt{7} \sqrt{8} \sqrt{9} \sqrt{10} \sqrt{11} \sqrt{12} \sqrt{13} \sqrt{14} \sqrt{15} \sqrt{16} \sqrt{17} \sqrt{18} \sqrt{19} \sqrt{20} \sqrt{21} \sqrt{22} \sqrt{23} \sqrt{24} $ $SPI_{MOSI} \_ \overline{RW} \sqrt{A6} \sqrt{A5} \sqrt{A4} \sqrt{A3} \sqrt{A2} \sqrt{A1} \sqrt{A0} \sqrt{X} \sqrt{X} \sqrt{X} \sqrt{X} \sqrt{X} \sqrt{X} \sqrt{X} X$
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18- 21-22.

'474 Patent Claim	Representative NXP Product(s)
	Multiple-byte read operations are performed similarly to single-byte reads with additional bytes read out in multiples of eight SCLK cycles. The register read address is auto- incremented by FXLS8962AF so that every eighth clock edge will latch the address of the next sequential register read address. When the desired number of bytes has been read, a rising edge on SPI_CS_B terminates the transaction.
	SPLCS_B
	SCLK1 2 3 4 5 6 7 7 6 1 6 1 7 1 2 1 3 1 4 1 5 1 6 1 7 1 8 1 6 20 2 1 2 2 2 2 2 4 2 6 2 7 2 9 2 9 2 9 3 1 5 2
	$spl_Mosi = - RW(Ab(Ab(Ab(Ab(Ab(Ab(X)(Ab(X)(X$
	SPI_MISO
	Figure 15. SPI multiple byte read protocol diagram (4-wire mode), R/W = 1
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18- 22.
	11.4 SPI read operations with 3-wire mode FXLS8962AF can be configured to operate in 3-wire software enabled SPI mode. In this mode, the SPI MISO pin is left unconnected and the SPI MOSI pin becomes a bidimeticated introduction (SPI DATA). Deed competition in 2-wire mode and the
	bidirectional input/output pin (SPI_DATA). Read operations in 3-wire mode are the same as write operations in 3- and 4-wire modes, except that at the end of the address cycle (falling edge of clock pulse 16), the SPI_DATA pin automatically switches from an input to an output and with bit D7 as the current output state.
	FXLS8962AF, 3-Axis Low-g Accelerometer, Product data sheet (Rev. 5.3 — 10 December 2019) at 18- 22.

'474 Patent Claim	Representative NXP Product(s)
	$[spl_cs_B] = [sc_K - (\sqrt{2}\sqrt{3}\sqrt{4}\sqrt{5}\sqrt{6}\sqrt{7}\sqrt{8}\sqrt{9}\sqrt{6}\sqrt{1}\sqrt{12}\sqrt{13}\sqrt{4}\sqrt{15}\sqrt{16}\sqrt{19}\sqrt{19}\sqrt{19}\sqrt{20}\sqrt{21}\sqrt{22}\sqrt{21}\sqrt{24}\sqrt{24}\sqrt{24}\sqrt{24}\sqrt{24}\sqrt{24}\sqrt{24}24$

'474 Patent Claim	Representative NXP Product(s)										
	1	4.3	Temperatur	re register	rő)						
	14.3.1 TEMP register (address 0x51)										
		F	Fight-bit 2's cr	omplement s	ensor temper	ature value v	with 0.96 °C.	/I SB sensitiv	vitv		
	Table 50. TEMP	P registe	er (address 0x)	51) bit allocat	tion						
	Bit	7	6	5	4	3	2	21	0		
	Symbol			0	die_tempe	rature[7:0]					
	Reset	0	0	0	0	0	0	0	0		
	Access	R	ĸ	R	ĸ	ĸ	R	ĸ	R	l	
	10.1.2 I <sup>2</sup> C re Singl The n the si	e-byte naster ave ad	rite operat read (or MCU) tra Idress, with	tions ansmits a s the R/W bi	start condition	on (ST) to t or a write,	he FXOS8 and the F>	3700CQ, fo	illowed by Q sends an		
	ackno	wledg	ement. The	n the mast	er (or MCU)	transmits	the addres	tor (or MCI	gister to		
	a repe	eated s	start conditio	on (SR), fol	lowed by th	e slave ad	dress with	the R/W b	it set to "1"		
	for a r	ead fro	om the prev	iously sele	cted registe	r. The FXC	S8700CQ	then ackn	owledges		
	and tr	ansmi	ts the data f	rom the rea	quested reg	ister. The r	master doe	es not ackn	owledge		
	(NAK	the tr	ansmitted d	ata, but tra	nsmits a st	op conditio	n to end th	e data trar	nsfer.		
	When	perfor	rming a mult	ti-byte or "b	urst" read,	the FXOS8	700CQ au	tomatically	increments		
	the re	gister	address rea	id pointer a	ifter a read	command i	s received	I. Therefore	e, after		
	follow	ing the	e steps of a	single-byte	read, multi	ple bytes o	f data can	be read fro	om		
	seque	ntial re	egisters afte	r each FX0	DS8700CQ	acknowled	gment (Ak	() is receive	ed until a no		
	ackno	ftranc	e (NAK) OCC	curs from th	e master fo	nowed by a	stop conc	attion (SP)	signaling an		
	endo	i ii alls	111351011.								

'474 Patent Claim	Representative NXP Product(s)
	FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer, Data sheet: Technical data (Rev. 8 — 25 April 2017) at 15.
	< Single-byte read >
	Master     ST     Device address[6:0]     W     Register address[7:0]     SR     Device address[6:0]     R     NAK     SP
	Slave AK AK AK Data[7:0]
	< Multiple-byte read >
	Master         ST         Device address[6:0]         W         Register address[7:0]         SR         Device address[6:0]         R         AK
	Slave AK AK Data[7:0]
	Master AK AK NAK SP
	Slave         Data[7:0]         Data[7:0]         Data[7:0]
	FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer, Data sheet: Technical data (Rev. 8 — 25 April 2017) at 16.
	10.2.2 SPI read/write operations
	A read operation is initiated by transmitting a 0 for the R/W bit. Then the 8-bit register
	address, ADDR[7:0] is encoded in the first and second serialized bytes. Subsequent bits are ignored by the part. The read data is deserialized from the MISO pin.
	FXOS8700CQ, 6-axis sensor with integrated linear accelerometer and magnetometer, Data sheet: Technical data (Rev. 8 — 25 April 2017) at 18.

'474 Patent Claim	Representative NXP Product(s)							
	1 General description							
	The FXPS7115D4 high-performance, high-precision barometric absolute pressure (BAP) sensor consists of a compact capacitive micro-electro-mechanical systems (MEMS) device coupled with a digital integrated circuit (IC) producing a fully calibrated digital output.							
	The sensor is based on NXP's high-precision capacitive pressure cell technology. The architecture benefits from redundant pressure transducers as an expanded quality measure. This sensor delivers highly accurate pressure and temperature readings through either a serial peripheral interface (SPI) or an inter-integrated circuit (I <sup>2</sup> C) interface. The FXPS7115D4 uses either a 3.3 V or 5.0 V power supply. Furthermore, the sensor employs an on-demand digital self-test for the digital IC and the MEMS transducers.							
	FXPS7115D4, Digital absolute pressure sensor, 40 kPa to 115 kPa, Product data sheet (Rev. 4 July 2020) at 1.	— 17						

'474 Patent Claim			Representativ	ve NXP Product(s)				
	7.3.4	Temperature senso	r					
	7.3.4.1	Temperature sensor s	ignal chain					
		The device includes a t Figure 12 shows a simp specified in <u>Table 104</u> a	emperature sensor for signa blified block diagram. Tempe and <u>Table 105</u> .	al compensation and user read erature sensor parameters are	ability.			
		temperature sensor CO		IVING OFFSET to temperature ( AND GAIN TRIM	023461			
		Figure 12. Temperature	e sensor signal chain block o	liagram				
	7.3.4.2	Temperature sensor output scaling equation						
		Table 8.	onvert temperature readings	s with the variables specified in				
			$T_{DEGC} = \frac{T_{LSB} - TO_{LS}}{T_{SENSE}}$	<u>u</u>	(5)			
		where:						
		T <sub>DEGC</sub> = The temper T <sub>LSB</sub> = The tempera	rature output in degrees C ture output in LSB	B at 0 °C				
		T <sub>SENSE</sub> = The expect	ted temperature sensitivity	in LSB/°C				
		Table 8. Temperature co	onversion variables					
		Data reading	TOLSB (LSB)	TSENSE LSB/C)				
		8-bit register read	68	1				

7.6 User-accessible data array         A user-accessible data array allows each device to be customized. The array consists of a one time programmable block, and CTP user-programmable block, and read-only registers for data and device status. The OTP blocks incorporate independent data verification.         Table 33. User-accessible data sensor specific information         Address Register       Type <sup>III</sup> Bit         Ceneral device information         Address Register       Type <sup>III</sup> Bit         Convrt_17:0)         ODH       COUNTIT: R       COUNTIT: R         ODH       COUNTIT: R       COUNTIT: R         ODH       COUNT R         ODH       COUNTIT: R         ODH       COUNTIT: R         ODH       COUNTIT: R         ODH       ODEVINIT         Address Figure Reserved       COUNTIT: R         COUNTIT: R       COUNTIT: R         ODH       COUNTIT: R         ODH       COUNTIT: R         ODH       COUNTIT: R			ct(s)	Produc	e NXP	entative	leprese	F				
Table 33. User-accessible data — sensor specific information         Address Register       Type <sup>(1)</sup> Bit         Control State       State         Type <sup>(1)</sup> Bit         Control State       State         Control State       State         Oth       COUNT       R       SUPPLY       TESTMODE       DEVRES       DEVINIT         Oth       COUNT       R       COUNT[7:0]         Oth       DEVSTAT       R       DSP_ERR       COUNT[7:0]         OTH       COUNT[7:0]       DEVISIT         ODh       DEVSTAT       R       DSP_ERR       COUNT[7:0]         OIP       DEVSTAT1       R       DSP_ERR       SUPPLY       TESTMODE       DEVRES       DEVINIT         02h       DEVSTAT1       R       VOCUV       ERR       ERR       ERR       ERR       ERR       ERR       ERR       ERR		onsists TP blocks	he array c OTP user- tus. The O	stomized. T block, an ( device stat	e to be cus grammable r data and	each devic actory-prog registers fo ation.	a array ray allows ble (OTP) f read-only lata verific	ble data ar rogramma block, and ependent of	er-accessi ser-accessi one time p grammable prporate ind	Us A u of a pro	7.6	
Address     Register     Type <sup>ITI</sup> Bit       7     6     5     4     3     2     1     0       General device information     COUNT     R     COUNT[7:0]     COUNT[7:0]       01h     DEVSTAT     R     DSP_ERR     reserved     COMM_ERR     MEMTEMP_ ERR     SUPPLY_ ERR     TESTMODE     DEVRES     DEVINIT       02h     DEVSTAT1     R     VCCUV_ ERR     reserved     COMM_ERR     MEMTEMP_ ERR     SUPPLY_ ERR     TESTMODE     DEVRES     DEVINIT       03h     DEVSTAT2     R     F_OTP_ERR     U_OTP_ ERR     U_W_ ERR     reserved     TEMP0_ ERR     reserved     reserved							informatio	or specific	data - sens	sible	3. User-acces	Table 3
7     6     5     4     3     2     1     0       General device information       00h     COUNT     R     COUNT[7:0]       01h     DEVSTAT     R     DSP_ERR     reserved     COMM_ERR     MEMTEMP_ ERR     SUPPLY_     TESTMODE     DEVRES     DEVINIT       02h     DEVSTAT1     R     VCCUV_ ERR     reserved     VCCOV_ ERR     reserved     INTREGA_ ERR     INTREGA_ ERR     INTREGA_ ERR     INTREGF_ ERR     CONT_ERR       03h     DEVSTAT2     R     F_OTP_ERR     U_OTP_ ERR     U_W_ ACTIVE     reserved     reserved     reserved     reserved					t:	BI			tul.	Туре	Register	Address
Ceneral device information       00h     COUNT     R     COUNT[7:0]       01h     DEVSTAT     R     DSP_ERR     reserved     COMM_ERR     MEMTEMP_ ERR     SUPPLY_ ERR     TESTMODE     DEVRES     DEVINIT       02h     DEVSTAT1     R     VCCUV_ ERR     reserved     VCCOV_ ERR     reserved     INTREGA_ ERR     INTREGA_ ERR     INTREGF_ ERR     CONT_ERR       03h     DEVSTAT2     R     F_OTP_ERR     U_OTP_ ERR     U_W_ ERR     reserved     reserved ERR     reserved ERR     reserved ERR     reserved		0	1	2	3	4	5	6	7			
Oth     DEVSTAT     R     DSP_ERR     reserved     COMM_ERR     METTEMP_ ERR     DSPLPLY_ ERR     TESTMODE     DEVRES     DEVINIT       02h     DEVSTAT1     R     VCCUV_ ERR     reserved     VCCOV_ ERR     reserved     INTREGA_ ERR     INTREGA_ ERR     INTREGF_ ERR     CONT_ERR       03h     DEVSTAT2     R     F_OTP_ERR     U_OTP_ ERR     U_W_ ERR     reserved     TEMP0_ ERR     reserved     reserved										1	device information	General
02h     DEVSTATI     R     VOCUV_ ERR     reserved     VOCOV_ ERR     reserved     INTREGA_ ERR     INTREGA_ ERR     INTREGF_ ERR     CONT_ERR       03h     DEVSTAT2     R     F_OTP_ERR     U_OTP_ ERR     U_W_ ERR     reserved     TEMPO_ ERR     reserved     reserved		DEVINIT	DEVRES	TESTMODE	SUPPLY	MEMTEMP	COMM ERR	reserved	DSP ERR	R	DEVSTAT	00h
02h     DEVSTATI     R     VCCUV_ ERR     reserved     VCCOV_ ERR     reserved     INTREG_ ERR     INTREG_ ERR     INTREG_ ERR     INTREG_ ERR     INTREG_ ERR     CONT_ERR       03h     DEVSTAT2     R     F_OTP_ERR     U_ORW_ERR     U_W ERR     reserved     TEMP0_ ERR     reserved     reserved					ERR	ERR				10°.		-
03h DEVSTAT2 R F_OTP_ERR U_OTP_ U_RW_ERR U_W reserved TEMP0_ reserved reserved reserved		CONT_ERR	INTREGF_	INTREG_ ERR	INTREGA_	reserved	VCCOV_	reserved	VCCUV_ ERR	R	DEVSTAT1	02h
LIN NOIVE EN		reserved	reserved	TEMP0_ ERR	reserved	U_W_ ACTIVE	U_RW_ERR	U_OTP_ ERR	F_OTP_ERR	R	DEVSTAT2	03h
04h DEVSTAT3 R MISO_ERR OSCTRAIN_ reserved reserved reserved reserved reserved reserved reserved reserved reserved		reserved	reserved	reserved	reserved	reserved	reserved	OSCTRAIN_ ERR	MISO_ERR	R	DEVSTAT3	04h
OSh reserved R reserved		reserved						R	reserved	05h		
OBh to reserved R reserved ODh		reserved						R	reserved	O6h to ODh		
DEh TEMPERATURE R TEMP[7:0]					[7:0]	TEMP				R	TEMPERATURE	OEh
OFn reserved R reserved					ved	reser			1	R	reserved	OFn

	Representative NXP Product(s)
	Representative NXP Product(s)         7.4.6.2 Register read transfers         The device supports I <sup>2</sup> C register read data transfers. Register read data transfers are constructed as follows:         1. The master transmits a START condition.       2. The master transmits the 7-bit slave address.         3. The master transmits a '0' for the read/write bit to indicate a write operation.       4. The slave transmits an ACK.         5. The master transmits the register address to be read.       6. The slave transmits an ACK.         7. The master transmits a repeat START condition.       8. The master transmits the 7-bit slave address.         9. The master transmits the 7-bit slave address.       9. The master transmits a '1' for the read/write bit to indicate a read operation.
F	<ul> <li>8. The master transmits the 7-bit slave address.</li> <li>9. The master transmits a '1' for the read/write bit to indicate a read operation.</li> <li>10. The slave transmits an ACK.</li> <li>11. The slave transmits the data from the register addressed.</li> <li>12. The master transmits a NACK.</li> <li>13. The master transmits a STOP condition.</li> </ul>

'474 Patent Claim	Representative NXP Product(s)							
	7.5.3	Command summary						
	7.5.3.1	Register read command						
		The device supports a register read command. The register read command uses the upper 7 bits of the addresses defined in <u>Section 7.6 "User-accessible data array"</u> to address 8-bit registers in the register map.						
		The response to a register read command is shown in <u>Section 7.5.3.1.2 "Register read</u> <u>response message format"</u> . The response is transmitted on the next SPI message if and only if all of the following conditions are met:						
		<ul> <li>No SPI error is detected (see Section 7.5.5.3 "SPI error")</li> <li>No MISO error is detected (see Section 7.5.5.4 "SPI data output verification error")</li> </ul>						
		If these conditions are met, the device responds to the register read request as shown in <u>Section 7.5.3.1.2 "Register read response message format"</u> . Otherwise, the device responds with the error response as defined in <u>Section 7.5.5.2 "Detailed status field"</u> . The register read response includes the register contents at the rising edge of SS_B for the register read command.						
	FXPS71 July 202	15D4, Digital absolute pressure sensor, 40 kPa to 115 kPa, Product data sheet (Rev. 4 — 17 0) at 20.						

'474 Patent Claim	Representative NXP Product(s)										
	7.5.3.1.1 Register read command message format										
	Table 13 Register read command message format										
	MSB: bit 31; LSB: bit 0										
	31 30 29 28 27 2										
	Command Fu C[3:0] m	ed bits: ist = 0h	Register address		Register data	8-bit CRC					
	1 1 0 0 0	0 0 0	RA[7:1]	RA[0]	0 0 0 0 0 0 0	CRC[7:0]					
		Table Bit fiel	14. Register read comma	and me	essage bit field descriptions						
		C[3:0]	Re	egister re	ad command = '1100'						
		RA[7:0	] R4	A[7:1] co	ntains the word address of the register	to be read.					
		CRC[7	:0] Re	ead CRC	Section						
	Table 15.         Register           MSB:         bit 31;         LSB:         bit           31         30         29         28         27										
	Command	eie Umus	Register	access	command	I I HA CDC					
	C[0], [3:1] Sta	tus Data	of RA[7:1] high byte	5	of RA[7:1] low byte	8-DIT CRC					
	0 1 1 0 ST[	1:0] 0	0 RD[15:8]		RD[7:0]	CRC[7:0]					
	FXPS7115D4, July 2020) at 2 Table 16. Rep Bit field	Digita 0. gister re	ad response messag	re se e bit	nsor, 40 kPa to 115	• kPa, Product data	sheet (Rev. 4 — 17				
	C[0], [3:1]		Register Read Command :	= '0110	!						
	ST[1:0]		Status								
	RD[15:8]		The contents of the registe	er addre	essed by RA[7:1] high byte (RA[	0] = 1)					
	RD[7:0]		The contents of the registe								
	CRC[7:0]		8-bit CRC								
	FXPS7115D4, July 2020) at 2	Digita 1.	l absolute pressu	re se	nsor, 40 kPa to 115	5 kPa, Product data	」 sheet (Rev. 4 — 17				

'474 Patent Claim	Representative NXP Product(s)							
[1a.] A serial communication system comprising:	To the extent the preamble is limiting, the Accused '474 Wireless Microcontrollers include a "serial communication system" as recited in the '474 patent. Exemplary systems and serial interfaces are identified in the block diagrams below.							
	See, e.g.,:							
	https://www.nxp.com/docs/en/data-sheet/K32W061.pdf See also https://www.avnet.com/shop/us/search/k32w041							
	OM15080-K32W (Development Board of K32W061/41)							
	https://www.arrow.com/en/products/om15080-k32w/nxp-semiconductors?q=OM15080-K32W							



'474 Patent Claim	Representative NXP Product(s)
	1.3 Block diagram         Image: state of the state
[1b.] an integrated circuit having a master serial interface; and	The Accused '474 Wireless Microcontrollers each includes an integrated circuit having a master serial interface. For example, the Accused '474 Wireless Microcontrollers each includes an integrated circuit having a master serial interface ( <i>e.g.</i> , the I2C interface on the master/MCU and/or the host processor).



74 Patent Claim	Representative NXP Product(s)
25.:	2 Features
<u> </u>	<ul> <li>Independent Master, Slave, and Monitor functions.</li> </ul>
	<ul> <li>Bus speeds supported:</li> </ul>
	<ul> <li>Standard mode, up to 100 kbits/s.</li> </ul>
	<ul> <li>Fast-mode, up to 400 kbits/s.</li> </ul>
	<ul> <li>Fast-mode Plus, up to 1 Mbits/s (on pins PIO0_10 and PIO0_11 that include specific I<sup>2</sup>C support).</li> </ul>
	<ul> <li>High speed mode, 3.4 Mbits/s as a Slave only (on pins PIO0_10 and PIO0_11 that include specific I<sup>2</sup>C support).</li> </ul>
	<ul> <li>Supports both Multi-master and Multi-master with Slave functions.</li> </ul>
	<ul> <li>Multiple I<sup>2</sup>C slave addresses supported in hardware.</li> </ul>
	<ul> <li>One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I<sup>2</sup>C bus addresses.</li> </ul>
	<ul> <li>10-bit addressing supported with software assist.</li> </ul>
	<ul> <li>Supports System Management Bus (SMBus).</li> </ul>
	<ul> <li>Separate DMA requests for Master, Slave, and Monitor functions.</li> </ul>
	<ul> <li>No chip clocks are required in order to receive and compare an address as a Slave, so this event can wake up the device from deep-sleep mode. Additionally, I<sup>2</sup>C0 can optionally generate a wake-up from power down.</li> </ul>
	<ul> <li>Automatic modes optionally allow less software overhead for some use cases.</li> </ul>



'474 Patent Claim	Representative NXP Product(s)							
	25.4.2.1       Slave read from master         This example uses polling to control the sequence and does not use interrupts. Configure the I <sup>2</sup> C as a slave with address x:         1.       Write the slave address x to the address 0 match register.         2.       Set the CFG[SLVEN] bit to 1.         K32W061/K32W041       User Manual, UM11323 (Rev. 1.1 — June 2020) at 173.							
[1c.] a processor having a slave serial interface coupled to the master serial interface through a clock signal line and a data signal line	The Accused '474 Wireless Microcontrollers each includes a processor having a slave serial interface coupled to the master serial interface through a clock signal line and a data signal line. For example, the Accused '474 Wireless Microcontrollers each includes a processor having a slave serial interface ( <i>e.g.</i> , I2C) coupled to the master serial interface identified above through a clock signal line ( <i>e.g.</i> , SCL) and a data signal line ( <i>e.g.</i> , SDA).							



'474 Patent Claim	Representative NXP Product(s)
	25.2 Features
	<ul> <li>Independent Master, Slave, and Monitor functions.</li> <li>Bus speeds supported: <ul> <li>Standard mode, up to 100 kbits/s.</li> <li>Fast-mode, up to 400 kbits/s.</li> <li>Fast-mode Plus, up to 1 Mbits/s (on pins PIO0_10 and PIO0_11 that include</li> </ul> </li> </ul>
	<ul> <li>specific I<sup>2</sup>C support).</li> <li>High speed mode, 3.4 Mbits/s as a Slave only (on pins PIO0_10 and PIO0_11 that include specific I<sup>2</sup>C support).</li> <li>Supports both Multi-master and Multi-master with Slave functions.</li> </ul>
	<ul> <li>Multiple I<sup>2</sup>C slave addresses supported in hardware.</li> <li>One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I<sup>2</sup>C bus addresses.</li> </ul>
	<ul> <li>10-bit addressing supported with software assist.</li> <li>Supports System Management Bus (SMBus).</li> <li>Separate DMA requests for Master, Slave, and Monitor functions.</li> </ul>
	<ul> <li>No chip clocks are required in order to receive and compare an address as a Slave, so this event can wake up the device from deep-sleep mode. Additionally, I<sup>2</sup>C0 can optionally generate a wake-up from power down.</li> </ul>
	<ul> <li>Automatic modes optionally allow less software overhead for some use cases.</li> </ul>
	K32W061/K32W041 User Manual, UM11323 (Rev. 1.1 — June 2020) at 170.



'474 Patent Claim	Representative NXP Product(s)
	25.4.2       I <sup>2</sup> C receive/transmit in slave mode In this example, I <sup>2</sup> C1 is used as an I <sup>2</sup> C slave. The slave receives 8 bits from the master and then sends 8 bits to the master. The SCL and SDA functions must be enabled on suitable pins, see Table 48.         The pins should be configured as required for the I <sup>2</sup> C-bus mode.         The transmission of the address and data bits is controlled by the STAT[SLVPENDING] status bit. Whenever the status is Slave pending, the slave can acknowledge ("ack") or send or receive an address and data. The received data or the data to be sent to the master are available in the SLVDAT register. After sending and receiving data, continue to the next step of the transmission protocol by writing to the SLVCTL register.         K32W061/K32W041 User Manual, UM11323 (Rev. 1.1 — June 2020) at 173.
	<ul> <li>25.4.2.1 Slave read from master This example uses polling to control the sequence and does not use interrupts. Configure the I<sup>2</sup>C as a slave with address x: <ol> <li>Write the slave address x to the address 0 match register.</li> <li>Set the CFG[SLVEN] bit to 1.</li> </ol> K32W061/K32W041 User Manual, UM11323 (Rev. 1.1 — June 2020) at 173.</li></ul>
[1d.] wherein the slave serial interface is responsive to a read temperature command issued by the master serial interface to return a temperature value associated with the processor.	In each of the Accused '474 Wireless Microcontrollers, the slave serial interface is responsive to a read temperature command issued by the master serial interface to return a temperature value associated with the processor. For example, in each of the Accused '474 Wireless Microcontrollers, the slave serial interface identified above is responsive to a read temperature command ( <i>e.g.</i> , the read tempearture command requesting the result derived from the temperature sensor measurement) issued by the identified master serial interface to return a temperature value ( <i>e.g.</i> , the result derived from the temperature sensor measurement) associated with the processor.

4 Patent Claim	Representative NXP Product(s)
25.4	.2.2 Slave write to master
	This example uses polling to control the sequence and does not use interrupts. Configure the I <sup>2</sup> C as a slave with address x:
	1. Write the slave address x to the address 0 match register.
	2. Set the CFG[SLVEN] bit to 1.
	Write data to the master:
	<ol> <li>Wait for the pending status to be set (STAT[SLVPENDING] = 1) by polling the STAT register. Check the status register STAT[SLVSTATE] indicating ADDR. If not then an error has occurred.</li> </ol>
	2. ACK the address by setting SLVCTL[SLVCONTINUE] = 1 in the slave control register.
	<ol> <li>Wait for the pending status to be set (STAT[SLVPENDING] = 1) by polling the STAT register. Check the status register STAT[SLVSTATE] is indicating TX. If not then an error has occurred.</li> </ol>
	4. Write 8 bits of data to SLVDAT register.
	<ol> <li>Continue the transaction by setting SLVCTL[SLVCONTINUE] = 1 in the slave control register.</li> </ol>

'474 Patent Claim	Representative NXP Product(s)	
	27.2 Features	
	<ul> <li>12-bit successive approximation analog to digital converter.</li> <li>Input multiplexing among up to 8 pins (6 external inputs, 1 temperature sensor and V<sub>BAT</sub>).</li> <li>A configurable conversion sequencer with configurable trigger</li> <li>Optional automatic high/low threshold comparison and "zero crossing" detection.</li> <li>12-bit conversion rate of 190 kHz. Options for reduced resolution at higher conversion rates.</li> <li>Burst conversion mode for single or multiple inputs.</li> <li>Asynchronous operation. Asynchronous mode allows choosing ADC clock from FRO12M or XO32M.</li> <li>A temperature sensor is connected to ADC channel 7, see <u>Chapter 28 "Temperature Sensor</u>" for further details.</li> <li>Supply monitor is connected to ADC channel 6; this monitors V<sub>BAT</sub>.</li> </ul>	
	<ul> <li>Configure the temperature sensor as follows:</li> <li>Select the temperature sensor as source for channel 7 of the ADC by writing the SEQ_CTRL[CHANNELS] bits to 0x80. In order to return ADC channel 7 to measuring its related device pin, write the SEQ_CTRL[CHANNELS] bits to 0x80.</li> <li>The digital temperature reading is available after an analog-to-digital conversion of</li> </ul>	
	ADC channel 7.  Remark: To convert the ADC conversion result into a temperature reading, use the API provided. This uses device specific calibration data stored in the device to increase the accuracy of the temperature reading.  K220W0(1/K220W0411U - M - 1 UM11222 (D - 1 1 - L - 2020) + 100	

'474 Patent Claim	Representative NXP Product(s)							
	Table 58. ADC channels							
	ADC channel	Function	Device Pin					
	0	ADC0	PIO14					
	1	ADC1	PIO15					
	2	ADC2	PIO16					
	3	ADC3	PIO17					
	4	ADC4	PIO18					
	5	ADC5	PIO19					
	6	Supply monitor	Internal function					
	7	Temperature sensor	Internal function					
	28.1 How to	UM113 Chapter 28: Rev. 1.1 — Jun o read this chapter	B23 Temperature Sensor ne 2020 Use er nsor is available on all K32W061/41 devices.	er manual				
		The temperature se	isor is available off all K32000 1/41 devices.					
	28.2 Featur	res						
		Linear temperat	ure sensor.					
		<ul> <li>Sensor output in</li> </ul>	nternally connected to the ADC channel 7 for temperature r	nonitoring				
	K32W061/K32	W041 User Manua	al, UM11323 (Rev. 1.1 — June 2020) at	208.				

	Representative NXP Product(s)
28.3	Basic configuration
	This section explains how the Temperature Sensor can be used. For a functional example see lpc_adc_basic.
	<ul> <li>Enable the power to the temperature sensor by setting the ASYNC_SYSCON_TEMPSENSORCTRL[ENABLE].</li> </ul>
	<ul> <li>Configure temperature sensor common mode output voltage setting ASYNC_SYSCON_TEMPSENSORCTRL[CM] = 0x2 for proper default operation</li> </ul>
	<ul> <li>To monitor the temperature continually, select the temperature sensor as source for channel 7 of ADC0. See <u>Chapter 27</u>. The digital temperature reading is available after an analog-to-digital conversion.</li> </ul>
	<ul> <li>The ADC reading must be converted into a temperature reading. To increase accuracy the sensor and ADC are calibrated during production, An API is provided to produce a temperature value; this performs the best configuration of the ADC for the purpose of the temperature sensor. The calibration data and other characteristics of the temperature and ADC are used to produce a high accuracy results.</li> </ul>
	<ul> <li>For highest accuracy, set ADCCLK mux source to be 32 MHz XTAL with a divider setting of 7, to give an ADCCLK of 4 MHz.</li> </ul>
	<ul> <li>The voltage range of operation of the ADC is set by ADC_GPADC_CTRL0[TEST]. In normal mode, the ADC can take an input voltage of 0 to 3.6 V, to V<sub>BAT</sub> if this is lower. For the temperature sensor, the ADC must be configured in Unity Gain mode when the input voltage range is 0 to 0.9 V. Since the temperature sensor voltage output is within this range, the best accuracy is achieved. A consequence of this is that the temperature sensor can not be combined with the other ADC inputs as part of sequencer configuration. Also, safe practice is to set the mode back to normal mode after using the ADC with the temperature sensor.</li> </ul>
K32W	)61/K32W041 User Manual, UM11323 (Rev. 1.1 — June 2020) at 208.
28.3.	Perform a single ADC conversion with the temperature sensor as ADC input

'474 Patent Claim	Representative NXP Product(s)
	To perform a single ADC conversion for ADC0 channel 7 using the temperature sensor output:
	1. Enable the temperature sensor output as input to ADC channel 7.
	2. Configure the system clock and the ADC for operation.
	3. Select the asynchronous mode in the ADC_CTRL register.
	<ol> <li>Select ADC channel 7 to perform the conversion by setting the ADC_SEQ_CTRL[CHANNELS] bits to 0x80.</li> </ol>
	5. Set the ADC_SEQ_CTRL[START] bit to 1.
	6. Read the SEQ_GDAT[RESULT] bits for the conversion result.
	<ol><li>The AHI software may be used to generate the temperature value. In fact, the example driver will perform this sequencing as well as making corrections due to the calibration data, and using averaging to give the best result.</li></ol>
	K32W061/K32W041 User Manual, UM11323 (Rev. 1.1 — June 2020) at 209.

'474 Patent Claim	Representative NXP Product(s)												
	17.1.3 ADC	Conver	sion Se	quence	Con	trol Reg	giste	er (Sl	EQ_0	CTR	L)		
	Register	Offset											
	SEQ_CTRL	8h											
	Function         This register controls triggering and channel selection for conversion sequence. Also specifies interrupt mode for sequence. All ADC conversions are controlled through this sequencer which can be used for a single conversion or sets of conversions on one or more channels.         Diagram												
	Bits 31 30	29 28	27 26	25 24	23	22 21	20	19	18	17	16		
	W ENA MODE	Reserv SINGL ed ES	BURS T STAR T	STAR T_B		Reserved		SYNC BYP	TRIGP OL	TRIG	GER		
	Reset 0 0	u 0	0 u	0 u	u	u u	u	0	0	0	0		
	Bits 15 14	13 12	11 10	9 8	7	6 5	4	3	2	1	0		
	W TRI	GGER	Res	erved			CHA	NNELS					
	Reset 0 0	0 0	u u	u u	0	0 0	0	0	0	0	0		
	K32W061/K32	W041 Reg	ister Man	ual (Rev	. 1.1,	06/2020)	at 44	0.				_	
	7-0 AE	C Channels											
	CHANNELS Select which one or more of the ADC channels will be sampled and converted when this sequence is launched. A 1 in any bit of this field will cause the corresponding channel to be included in the conversion sequence, where bit 0 corresponds to channel 0, bit 1 to channel 1 and so forth. Bit 6 is channel 6; the supply monitor. Bit 7 is channel 7; the temperature sensor. When this conversion sequence is triggered, either by a hardware trigger or via software command, ADC conversions will be performed on each enabled channel, in sequence, beginning with the lowest-ordered channel. Remark: This field can ONLY be changed while SEQ_ENA (bit 31) is LOW. It is allowed to change this field and set bit 31 in the same write.								ilon d, iled ged				

'474 Patent Claim	Representative NXP Product(s)		
	17.1.4 AD	C Sequence Global Data Register (SEQ_GDAT)	
	Register	Offset	
	SEQ_GDAT	10h	
	Function This register contains the result of the most recent ADC conversion completed under each conversion sequence. Results of ADC conversions can be read in one of two ways. One is to use this register to read data from the ADC at the end of each ADC conversion. The other is to read the individual ADC Channel Data (DATn) registers, typically after the entire sequence has completed. It is recommended to use one method consistently for a given conversion sequence. This register is useful in conjunction with DMA operation - particularly when the channels selected for conversion are not sequential (hence the addresses of the individual result registers will not be sequential, making it difficult for the DMA engine to address them). For interrupt-driven code, it will more likely be advantageous to wait for an entire sequence to complete and then retrieve the results from the individual channel registers. NOTE The method to be employed for each sequence should be reflected in the SEQ_CTRL[MODE] bit since this will		
	K32W061/K	ADC Conversion Result This field contains the 12-bit ADC conversion result from the most recent conversion performed under conversion sequence associated with this register. DATAVALID = 1 indicates that this result has not yet been read. If less than 12-bit resolution is used the ADC result occupies the upper MSBs and unused LSBs should be ignored. 32W041 Register Manual (Rev. 1.1, 06/2020) at 445.	

'474 Patent Claim	Representative NXP Product(s)		
	17.1.5 AD	OC Channel a Data Register (DAT0 - DAT7)	
	Function		
	These registers h when a conversio to the range dicta	old the result of the last conversion completed for each ADC channel. They also include status bits to indicate in has been completed, when a data overrun has occurred, and where the most recent conversion fits relative ted by the high and low threshold registers.	
	Results of ADC or read data from the typically after the sequence.	onversion can be read in one of two ways. One is to use the SEQ_GDAT register for each of the sequences to e ADC at the end of each ADC conversion. The other is to use these individual ADC Channel Data registers, entire sequence has completed. It is recommended to use one method consistently for a given conversion	
		NOTE	
	The	method to be employed for each sequence should be reflected in the MODE bit in the SEQ_CTRL register e this will impact interrupt and overrun flag generation.	
	The information p regardless of what	resented in the DAT registers always pertains to the most recent conversion completed on that channel at sequence requested the conversion or which trigger caused it.	
	The OVERRUN fi	elds for each channel are also replicated in the FLAGS register.	
	K32W061/K	32W041 Register Manual (Rev. 1.1, 06/2020) at 445-446.	
	15-4	ADC Conversion Result	
	RESULT	This field contains the 12-bit ADC conversion result from the most recent conversion performed under conversion sequence associated with this register. DATAVALID = 1 indicates that this result has not yet been read. If less than 12-bit resolution is used, the ADC result occupies the upper MSBs and unused LSBs should be ignored.	
	K32W061/K See also:	+ 32W041 Register Manual (Rev. 1.1, 06/2020) at 447.	

Representative NXP Product(s)			
Application sends       Temperature update         to radio driver       VR-adio_Temp_         VR-adio_Temp_       Update() API         Temperature       Temperature         VR-adio_Temp_       Update() API         Temperature       NOREG1 always on register         Temperature       Fig 142. Communication between application / MAC SW and Radio SW driver         K32W061/K32W041 User Manual, UM11323 (Rev. 1.1 — June 2020) at 324.			
To the extent the preamble is limiting, the Accused '474 Wireless Microcontrollers perform a method for communicating over a point to point serial communication system having a clock signal line and a data signal line coupling a serial interface master and a serial interface slave. For example, each of the Accused '474 Wireless Microcontrollers perform a method for communicating over a point to point serial communication system identified below having a clock signal line ( <i>e.g.</i> , SCL) and a data signal line ( <i>e.g.</i> , SDA) coupling a serial interface master ( <i>e.g.</i> , the I2C interface on the master/MCU and/or the host processor) and a serial interface slave ( <i>e.g.</i> , I2C). See, e.g.:			
https://www.nxp.com/docs/en/data-sheet/K32W061.pdf See also https://www.avnet.com/shop/us/search/k32w041			

'474 Patent Claim	Representative NXP Product(s)	
	OM15080-K32W (Development Board of K32W061/41)	
	https://www.arrow.com/en/products/om15080-k32w/nxp-semiconductors?q=OM15080-K32W	




'474 Patent Claim	Representative NXP Product(s)			
	25.2 Features			
	<ul> <li>Independent Master, Slave, and Monitor functions.</li> <li>Bus speeds supported: <ul> <li>Standard mode, up to 100 kbits/s.</li> <li>Fast-mode, up to 400 kbits/s.</li> <li>Fast-mode Plus, up to 1 Mbits/s (on pins PIO0_10 and PIO0_11 that include</li> </ul> </li> </ul>			
	<ul> <li>specific I<sup>2</sup>C support).</li> <li>High speed mode, 3.4 Mbits/s as a Slave only (on pins PIO0_10 and PIO0_11 that include specific I<sup>2</sup>C support).</li> <li>Supports both Multi-master and Multi-master with Slave functions.</li> </ul>			
	<ul> <li>Multiple I<sup>2</sup>C slave addresses supported in hardware.</li> <li>One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I<sup>2</sup>C bus addresses.</li> </ul>			
	<ul> <li>10-bit addressing supported with software assist.</li> <li>Supports System Management Bus (SMBus).</li> <li>Separate DMA requests for Master, Slave, and Monitor functions.</li> </ul>			
	<ul> <li>No chip clocks are required in order to receive and compare an address as a Slave, so this event can wake up the device from deep-sleep mode. Additionally, I<sup>2</sup>C0 can optionally generate a wake-up from power down.</li> </ul>			
	<ul> <li>Automatic modes optionally allow less software overhead for some use cases.</li> </ul>			
	K32W061/K32W041 User Manual, UM11323 (Rev. 1.1 — June 2020) at 170.			



'474 Patent Claim	Representative NXP Product(s)
	<ul> <li>25.4.2 I<sup>2</sup>C receive/transmit in slave mode In this example, I<sup>2</sup>C1 is used as an I<sup>2</sup>C slave. The slave receives 8 bits from the master and then sends 8 bits to the master. The SCL and SDA functions must be enabled on suitable pins, see Table 48. The pins should be configured as required for the I<sup>2</sup>C-bus mode. The transmission of the address and data bits is controlled by the STAT[SLVPENDING] status bit. Whenever the status is Slave pending, the slave can acknowledge ("ack") or send or receive an address and data. The received data or the data to be sent to the master are available in the SLVDAT register. After sending and receiving data, continue to the next step of the transmission protocol by writing to the SLVCTL register.</li> </ul> K32W061/K32W041 User Manual, UM11323 (Rev. 1.1 — June 2020) at 173.
	25.4.2.1       Slave read from master         This example uses polling to control the sequence and does not use interrupts. Configure the I <sup>2</sup> C as a slave with address x:         1.       Write the slave address x to the address 0 match register.         2.       Set the CFG[SLVEN] bit to 1.         K32W061/K32W041 User Manual, UM11323 (Rev. 1.1 — June 2020) at 173.
[8b.] sending a read temperature command to the serial interface slave from the serial interface master using the clock signal line and the data signal line; and	The Accused '474 Wireless Microcontrollers performs a step of sending a read temperature command to the serial interface slave from the serial interface master using the clock signal line and the data signal line. For example, each of the Accused '474 Wireless Microcontrollers perform a step of sending a read temperature command ( <i>e.g.</i> , the read tempearture command requesting the result derived from the temperature sensor measurement) to the serial interface slave identified above from the serial interface master identified above using the clock signal line identified above and the data signal line identified above.

Patent Claim	Representative NXP Product(s)
25	12.2 Slave write to master
23.	This example uses polling to control the sequence and does not use interrupts. Configure the I <sup>2</sup> C as a slave with address x:
	1. Write the slave address x to the address 0 match register.
	2. Set the CFG[SLVEN] bit to 1.
	Write data to the master:
	<ol> <li>Wait for the pending status to be set (STAT[SLVPENDING] = 1) by polling the STAT register. Check the status register STAT[SLVSTATE] indicating ADDR. If not then an error has occurred.</li> </ol>
	2. ACK the address by setting SLVCTL[SLVCONTINUE] = 1 in the slave control register.
	<ol> <li>Wait for the pending status to be set (STAT[SLVPENDING] = 1) by polling the STAT register. Check the status register STAT[SLVSTATE] is indicating TX. If not then an error has occurred.</li> </ol>
	4. Write 8 bits of data to SLVDAT register.
	<ol> <li>Continue the transaction by setting SLVCTL[SLVCONTINUE] = 1 in the slave control register.</li> </ol>

'474 Patent Claim	Representative NXP Product(s)	
	27.2 Features	
	<ul> <li>12-bit successive approximation analog to digital converter.</li> <li>Input multiplexing among up to 8 pins (6 external inputs, 1 temperature sensor and V<sub>BAT</sub>).</li> <li>A configurable conversion sequencer with configurable trigger</li> <li>Optional automatic high/low threshold comparison and "zero crossing" detection.</li> <li>12-bit conversion rate of 190 kHz. Options for reduced resolution at higher conversion rates.</li> <li>Burst conversion mode for single or multiple inputs.</li> <li>Asynchronous operation. Asynchronous mode allows choosing ADC clock from FRO12M or XO32M.</li> <li>A temperature sensor is connected to ADC channel 7, see <u>Chapter 28 "Temperature Sensor</u>" for further details.</li> <li>Supply monitor is connected to ADC channel 6; this monitors V<sub>BAT</sub>.</li> </ul>	
	<ul> <li>Configure the temperature sensor as follows:</li> <li>Select the temperature sensor as source for channel 7 of the ADC by writing the SEQ_CTRL[CHANNELS] bits to 0x80. In order to return ADC channel 7 to measuring its related device pin, write the SEQ_CTRL[CHANNELS] bits to 0x80.</li> <li>The digital temperature reading is available after an analog-to-digital conversion of</li> </ul>	
	ADC channel 7.  Remark: To convert the ADC conversion result into a temperature reading, use the API provided. This uses device specific calibration data stored in the device to increase the accuracy of the temperature reading.  K220W0(1/K220W0411U - M - 1 UM11222 (D - 1 1 - L - 2020) + 100	

'474 Patent Claim			Representative NXP Product(s	)
	Table 58. ADC	channels		
	ADC channel	Function	Device Pin	
	0	ADC0	PIO14	
	1	ADC1	PIO15	
	2	ADC2	PIO16	
	3	ADC3	PIO17	
	4	ADC4	PIO18	
	5	ADC5	PIO19	
	6	Supply monitor	Internal function	
	7	Temperature sensor	Internal function	
	28.1 How to	UM113 Chapter 28: Rev. 1.1 — Ju	323 Temperature Sensor ne 2020 er	User manual
		The temperature se		
	28.2 Featur	res		
		Linear tempera	ture sensor.	
		Sensor output i	nternally connected to the ADC channel 7 for ter	nperature monitoring
	K32W061/K32	W041 User Manua	al, UM11323 (Rev. 1.1 — June 2	020) at 208.

	Representative NXP Product(s)
28.3	Basic configuration
	This section explains how the Temperature Sensor can be used. For a functional example see lpc_adc_basic.
	<ul> <li>Enable the power to the temperature sensor by setting the ASYNC_SYSCON_TEMPSENSORCTRL[ENABLE].</li> </ul>
	<ul> <li>Configure temperature sensor common mode output voltage setting ASYNC_SYSCON_TEMPSENSORCTRL[CM] = 0x2 for proper default operation</li> </ul>
	<ul> <li>To monitor the temperature continually, select the temperature sensor as source for channel 7 of ADC0. See <u>Chapter 27</u>. The digital temperature reading is available after an analog-to-digital conversion.</li> </ul>
	<ul> <li>The ADC reading must be converted into a temperature reading. To increase accuracy the sensor and ADC are calibrated during production, An API is provided to produce a temperature value; this performs the best configuration of the ADC for the purpose of the temperature sensor. The calibration data and other characteristics of the temperature and ADC are used to produce a high accuracy results.</li> </ul>
	<ul> <li>For highest accuracy, set ADCCLK mux source to be 32 MHz XTAL with a divider setting of 7, to give an ADCCLK of 4 MHz.</li> </ul>
	<ul> <li>The voltage range of operation of the ADC is set by ADC_GPADC_CTRL0[TEST]. In normal mode, the ADC can take an input voltage of 0 to 3.6 V, to V<sub>BAT</sub> if this is lower. For the temperature sensor, the ADC must be configured in Unity Gain mode when the input voltage range is 0 to 0.9 V. Since the temperature sensor voltage output is within this range, the best accuracy is achieved. A consequence of this is that the temperature sensor can not be combined with the other ADC inputs as part of sequencer configuration. Also, safe practice is to set the mode back to normal mode after using the ADC with the temperature sensor.</li> </ul>
K32W	)61/K32W041 User Manual, UM11323 (Rev. 1.1 — June 2020) at 208.
28.3.	Perform a single ADC conversion with the temperature sensor as ADC input

'474 Patent Claim	Representative NXP Product(s)
	To perform a single ADC conversion for ADC0 channel 7 using the temperature sensor output:
	1. Enable the temperature sensor output as input to ADC channel 7.
	2. Configure the system clock and the ADC for operation.
	3. Select the asynchronous mode in the ADC_CTRL register.
	<ol> <li>Select ADC channel 7 to perform the conversion by setting the ADC_SEQ_CTRL[CHANNELS] bits to 0x80.</li> </ol>
	5. Set the ADC_SEQ_CTRL[START] bit to 1.
	6. Read the SEQ_GDAT[RESULT] bits for the conversion result.
	7. The AHI software may be used to generate the temperature value. In fact, the example driver will perform this sequencing as well as making corrections due to the calibration data, and using averaging to give the best result.
	K32W061/K32W041 User Manual, UM11323 (Rev. 1.1 — June 2020) at 209.

'474 Patent Claim	Representative NXP Product(s)												
	17.1.3 ADC	Conver	sion Se	quence	Con	trol Reg	giste	er (Sl	EQ_0	CTR	L)		
	Register	Offset											
	SEQ_CTRL	8h											
	Function         This register controls triggering and channel selection for conversion sequence. Also specifies interrupt mode for sequence. All ADC conversions are controlled through this sequencer which can be used for a single conversion or sets of conversions on one or more channels.         Diagram												
	Bits 31 30	29 28	27 26	25 24	23	22 21	20	19	18	17	16		
	W ENA MODE	Reserv SINGL ed ES	BURS T STAR T	STAR T_B		Reserved		SYNC BYP	TRIGP OL	TRIG	GER		
	Reset 0 0	u 0	0 u	0 u	u	u u	u	0	0	0	0		
	Bits 15 14	13 12	11 10	9 8	7	6 5	4	3	2	1	0		
	W TRI	GGER	Res	erved			CHA	NNELS					
	Reset 0 0	0 0	u u	u u	0	0 0	0	0	0	0	0		
	K32W061/K32	W041 Reg	ister Man	ual (Rev	. 1.1,	06/2020)	at 44	0.				_	
	7-0 AE	C Channels											
CHANNELS Select which one or more of the ADC channels will be sampled and converted when this sequence is launched. A 1 in any bit of this field will cause the corresponding channel to be included in the conversion sequence, where bit 0 corresponds to channel 0, bit 1 to channel 1 and so forth. Bit 6 is channel 6; the supply monitor. Bit 7 is channel 7; the temperature sensor. When this conversion sequence is triggered, either by a hardware trigger or via software command, ADC conversions will be performed on each enabled channel, in sequence, beginning with the lowest-ordered channel. Remark: This field can ONLY be changed while SEQ_ENA (bit 31) is LOW. It is allowed to change this field and set bit 31 in the same write.						ilon d, iled ged							

'474 Patent Claim		Representative NXP Product(s)	
	17.1.4 AC	C Sequence Global Data Register (SEQ_GDAT)	
	Register	Offset	
	SEQ_GDAT	10h	
	Function		
	This register conta conversions can b conversion. The o completed. It is rea	ins the result of the most recent ADC conversion completed under each conversion sequence. Results of ADC e read in one of two ways. One is to use this register to read data from the ADC at the end of each ADC ther is to read the individual ADC Channel Data (DATn) registers, typically after the entire sequence has commended to use one method consistently for a given conversion sequence.	
	This register is use sequential (hence address them). Fo retrieve the results	eful in conjunction with DMA operation - particularly when the channels selected for conversion are not the addresses of the individual result registers will not be sequential, making it difficult for the DMA engine to r interrupt-driven code, it will more likely be advantageous to wait for an entire sequence to complete and then s from the individual channel registers.	
		NOTE	
	The r impa	nethod to be employed for each sequence should be reflected in the SEQ_CTRL[MODE] bit since this will t interrupt and overrun flag generation.	
	K32W061/K	32W041 Register Manual (Rev. 1.1, 06/2020) at 443.	
	15-4	ADC Conversion Result	
	RESULT	This field contains the 12-bit ADC conversion result from the most recent conversion performed under conversion sequence associated with this register. DATAVALID = 1 indicates that this result has not yet been read. If less than 12-bit resolution is used the ADC result occupies the upper MSBs and unused LSBs should be ignored.	
	K32W061/K	32W041 Register Manual (Rev. 1.1, 06/2020) at 445.	

'474 Patent Claim	Representative NXP Product(s)					
	17.1.5 AD	OC Channel a Data Register (DAT0 - DAT7)				
	Function					
	These registers h when a conversio to the range dicta	old the result of the last conversion completed for each ADC channel. They also include status bits to indicate in has been completed, when a data overrun has occurred, and where the most recent conversion fits relative ted by the high and low threshold registers.				
	Results of ADC or read data from the typically after the sequence.	onversion can be read in one of two ways. One is to use the SEQ_GDAT register for each of the sequences to e ADC at the end of each ADC conversion. The other is to use these individual ADC Channel Data registers, entire sequence has completed. It is recommended to use one method consistently for a given conversion				
		NOTE				
	The	method to be employed for each sequence should be reflected in the MODE bit in the SEQ_CTRL register e this will impact interrupt and overrun flag generation.				
	The information p regardless of what	resented in the DAT registers always pertains to the most recent conversion completed on that channel at sequence requested the conversion or which trigger caused it.				
	The OVERRUN fi	ields for each channel are also replicated in the FLAGS register.				
	K32W061/K	32W041 Register Manual (Rev. 1.1, 06/2020) at 445-446.				
	15-4	ADC Conversion Result				
	RESULT	This field contains the 12-bit ADC conversion result from the most recent conversion performed under conversion sequence associated with this register. DATAVALID = 1 indicates that this result has not yet been read. If less than 12-bit resolution is used, the ADC result occupies the upper MSBs and unused LSBs should be ignored.				
	K32W061/K See also:	+ 32W041 Register Manual (Rev. 1.1, 06/2020) at 447.				

'474 Patent Claim	Representative NXP Product(s)						
	Application sends       Temperature update         to radio driver       Temperature         vPacific_Temp       update         Image: Temperature       Initial calibration         Not       Beeded?         Image: Temperature       Initial calibration         Not       Function         Image: Temperature       AOREG1 always on register         Temperature       Function         Fig 142. Communication between application / MAC SW and Radio SW driver         K32W061/K32W041 User Manual, UM11323 (Rev. 1.1 — June 2020) at 324.						
[8c.] in response to the read temperature command, the serial interface slave supplying over the data signal line a temperature value associated with a processor on an integrated circuit containing the serial interface slave.	The Accused '474 Wireless Microcontrollers performs a step of in response to the read temperature command, the serial interface slave supplying over the data signal line a temperature value associated with a processor on an integrated circuit containing the serial interface slave. For example, each of the Accused '474 Wireless Microcontrollers perform a step of in response to the read temperature command, the serial interface slave (e.g., the serial interface slave identified above in [8b.]) supplying over the data signal line (e.g., the data signal identified above in [8b.]) a temperature value associated with a processor on an integrated circuit containing the serial interface slave (e.g., the result derived from the temperature sensor measurement).						

'474 Patent Claim	Representative NXP Product(s)	
	25.4.2.2 Slave write to master	
	This example uses polling to control the sequence and does not use interrupts. Co the I <sup>2</sup> C as a slave with address x:	nfigure
	1. Write the slave address x to the address 0 match register.	
	2. Set the CFG[SLVEN] bit to 1.	
	Write data to the master:	
	<ol> <li>Wait for the pending status to be set (STAT[SLVPENDING] = 1) by polling the register. Check the status register STAT[SLVSTATE] indicating ADDR. If not th error has occurred.</li> </ol>	STAT Jen an
	2. ACK the address by setting SLVCTL[SLVCONTINUE] = 1 in the slave control n	egister.
	<ol> <li>Wait for the pending status to be set (STAT[SLVPENDING] = 1) by polling the register. Check the status register STAT[SLVSTATE] is indicating TX. If not the error has occurred.</li> </ol>	STAT In an
	4. Write 8 bits of data to SLVDAT register.	
	<ol><li>Continue the transaction by setting SLVCTL[SLVCONTINUE] = 1 in the slave register.</li></ol>	control
	32W061/K32W041 User Manual, UM11323 (Rev. 1.1 — June 2020) at 174.	

'474 Patent Claim	Representative NXP Product(s)	
	27.2 Features	
	<ul> <li>12-bit successive approximation analog to digital converter.</li> <li>Input multiplexing among up to 8 pins (6 external inputs, 1 temperature sensor and V<sub>BAT</sub>).</li> <li>A configurable conversion sequencer with configurable trigger</li> <li>Optional automatic high/low threshold comparison and "zero crossing" detection.</li> <li>12-bit conversion rate of 190 kHz. Options for reduced resolution at higher conversion rates.</li> <li>Burst conversion mode for single or multiple inputs.</li> <li>Asynchronous operation. Asynchronous mode allows choosing ADC clock from FRO12M or XO32M.</li> <li>A temperature sensor is connected to ADC channel 7, see <u>Chapter 28 "Temperature Sensor"</u> for further details.</li> <li>Supply monitor is connected to ADC channel 6; this monitors V<sub>BAT</sub>.</li> </ul>	
	<ul> <li>Configure the temperature sensor as follows:</li> <li>Select the temperature sensor as source for channel 7 of the ADC by writing the SEQ_CTRL[CHANNELS] bits to 0x80. In order to return ADC channel 7 to measuring its related device pin, write the SEQ_CTRL[CHANNELS] bits to 0x80.</li> <li>The digital temperature reading is available after an analog-to-digital conversion of</li> </ul>	
	ADC channel 7. Remark: To convert the ADC conversion result into a temperature reading, use the API provided. This uses device specific calibration data stored in the device to increase the accuracy of the temperature reading. K32W061/K32W041 User Manual, UM11323 (Rev. 1.1 — June 2020) at 199.	

'474 Patent Claim			Representative NXP Product(s)	
	Table 58. ADC	channels		
	ADC channel	Function	Device Pin	
	0	ADC0	PIO14	
	1	ADC1	PIO15	
	2	ADC2	PIO16	
	3	ADC3	PIO17	
	4	ADC4	PIO18	
	5	ADC5	PIO19	
	6	Supply monitor	Internal function	
	7	Temperature sensor	Internal function	
	28.1 How to	UM113 Chapter 28: Rev. 1.1 — Jun o read this chapter	B23 Temperature Sensor ne 2020 Use er nsor is available on all K32W061/41 devices.	er manual
		The temperature se	isor is available off all K32000 1/41 devices.	
	28.2 Featur	res		
		Linear temperat	ure sensor.	
		<ul> <li>Sensor output in</li> </ul>	nternally connected to the ADC channel 7 for temperature r	nonitoring
	K32W061/K32	W041 User Manua	al, UM11323 (Rev. 1.1 — June 2020) at	208.

	Representative NXP Product(s)
28.3	Basic configuration
	This section explains how the Temperature Sensor can be used. For a functional example see lpc_adc_basic.
	<ul> <li>Enable the power to the temperature sensor by setting the ASYNC_SYSCON_TEMPSENSORCTRL[ENABLE].</li> </ul>
	<ul> <li>Configure temperature sensor common mode output voltage setting ASYNC_SYSCON_TEMPSENSORCTRL[CM] = 0x2 for proper default operation</li> </ul>
	<ul> <li>To monitor the temperature continually, select the temperature sensor as source for channel 7 of ADC0. See <u>Chapter 27</u>. The digital temperature reading is available after an analog-to-digital conversion.</li> </ul>
	<ul> <li>The ADC reading must be converted into a temperature reading. To increase accuracy the sensor and ADC are calibrated during production, An API is provided to produce a temperature value; this performs the best configuration of the ADC for the purpose of the temperature sensor. The calibration data and other characteristics of the temperature and ADC are used to produce a high accuracy results.</li> </ul>
	<ul> <li>For highest accuracy, set ADCCLK mux source to be 32 MHz XTAL with a divider setting of 7, to give an ADCCLK of 4 MHz.</li> </ul>
	<ul> <li>The voltage range of operation of the ADC is set by ADC_GPADC_CTRL0[TEST]. In normal mode, the ADC can take an input voltage of 0 to 3.6 V, to V<sub>BAT</sub> if this is lower. For the temperature sensor, the ADC must be configured in Unity Gain mode when the input voltage range is 0 to 0.9 V. Since the temperature sensor voltage output is within this range, the best accuracy is achieved. A consequence of this is that the temperature sensor can not be combined with the other ADC inputs as part of sequencer configuration. Also, safe practice is to set the mode back to normal mode after using the ADC with the temperature sensor.</li> </ul>
K32W	)61/K32W041 User Manual, UM11323 (Rev. 1.1 — June 2020) at 208.
28.3.	Perform a single ADC conversion with the temperature sensor as ADC input

'474 Patent Claim	Representative NXP Product(s)
	To perform a single ADC conversion for ADC0 channel 7 using the temperature sensor output:
	1. Enable the temperature sensor output as input to ADC channel 7.
	2. Configure the system clock and the ADC for operation.
	3. Select the asynchronous mode in the ADC_CTRL register.
	<ol> <li>Select ADC channel 7 to perform the conversion by setting the ADC_SEQ_CTRL[CHANNELS] bits to 0x80.</li> </ol>
	5. Set the ADC_SEQ_CTRL[START] bit to 1.
	<ol><li>Read the SEQ_GDAT[RESULT] bits for the conversion result.</li></ol>
	7. The AHI software may be used to generate the temperature value. In fact, the example driver will perform this sequencing as well as making corrections due to the calibration data, and using averaging to give the best result.
	K32W061/K32W041 User Manual, UM11323 (Rev. 1.1 — June 2020) at 209.

'474 Patent Claim				Represe	ntativ	e NXP Pı	oduc	et(s)					
	17.1.3 ADC	Conver	sion Se	quence	Con	trol Reg	giste	er (Sl	EQ_0	CTR	L)		
	Register	Offset											
	SEQ_CTRL	8h											
	Function This register controls ADC conversions are or more channels. Diagram	triggering and o	channel selecti ugh this sequer	on for conver ncer which ca	ion sequ be used	ence. Also spe I for a single co	ecifies ir nversio	nterrupt i n or sets	mode for s of conv	r seque ersions	ence. <mark>All</mark> s on one		
	Bits 31 30	29 28	27 26	25 24	23	22 21	20	19	18	17	16		
	W ENA MODE	Reserv SINGL ed ES	BURS T STAR T	STAR T_B		Reserved		SYNC BYP	TRIGP OL	TRIG	GER		
	Reset 0 0	u 0	0 u	0 u	u	u u	u	0	0	0	0		
	Bits 15 14	13 12	11 10	9 8	7	6 5	4	3	2	1	0		
	W TRI	GGER	Res	erved			CHA	NNELS					
	Reset 0 0	0 0	u u	u u	0	0 0	0	0	0	0	0		
	K32W061/K32	W041 Reg	ister Man	ual (Rev	. 1.1,	06/2020)	at 44	0.				_	
	7-0 AE	C Channels											
	CHANNELS Se lau se su eitl ch wh	lect which one inched. A 1 in a quence, where pply monitor. B her by a hardwa annel, in seque ile SEQ_ENA	or more of the any bit of this bit 0 correspo- it 7 is channe are trigger or v nce, beginnin (bit 31) is LOV	e ADC chan field will cau onds to chan I 7; the temp ria software o g with the low V. It is allow	nels will l se the co nel 0, bit erature s ommand est-orde ed to cha	be sampled a prresponding 1 to channel sensor. When d, ADC conve ared channel. I ange this field	nd con channe 1 and this co rsions v Remark and se	verted v el to be i so forth onversio will be p k: This fi et bit 31	when thi included b. Bit 6 is on seque erforme ield can in the s	is sequ d in the s chann ence is d on ea ONLY ame w	ence is convers nel 6; the triggere ach enab be chan rite.	ilon d, iled ged	

'474 Patent Claim		Representative NXP Product(s)	
	17.1.4 AE	C Sequence Global Data Register (SEQ_GDAT)	
	Register	Offset	
	SEQ_GDAT	10h	
	Function		
	This register conta conversions can b conversion. The o completed. It is re	ins the result of the most recent ADC conversion completed under each conversion sequence. Results of ADC e read in one of two ways. One is to use this register to read data from the ADC at the end of each ADC ther is to read the individual ADC Channel Data (DATn) registers, typically after the entire sequence has commended to use one method consistently for a given conversion sequence.	
	This register is us sequential (hence address them). For retrieve the results	eful in conjunction with DMA operation - particularly when the channels selected for conversion are not the addresses of the individual result registers will not be sequential, making it difficult for the DMA engine to r interrupt-driven code, it will more likely be advantageous to wait for an entire sequence to complete and then s from the individual channel registers.	
	The i impa	NOTE method to be employed for each sequence should be reflected in the SEQ_CTRL[MODE] bit since this will ct interrupt and overrun flag generation.	
	K32W061/K	C32W041 Register Manual (Rev. 1.1, 06/2020) at 443.	
	15-4	ADC Conversion Result	
	RESULT	This field contains the 12-bit ADC conversion result from the most recent conversion performed under conversion sequence associated with this register. DATAVALID = 1 indicates that this result has not yet been read. If less than 12-bit resolution is used the ADC result occupies the upper MSBs and unused LSBs should be ignored.	
	K32W061/K	32W041 Register Manual (Rev. 1.1, 06/2020) at 445.	

'474 Patent Claim		Representative NXP Product(s)				
	17.1.5 AD	OC Channel a Data Register (DAT0 - DAT7)				
	Function					
	These registers h when a conversio to the range dicta	old the result of the last conversion completed for each ADC channel. They also include status bits to indicate in has been completed, when a data overrun has occurred, and where the most recent conversion fits relative ted by the high and low threshold registers.				
	Results of ADC or read data from the typically after the sequence.	onversion can be read in one of two ways. One is to use the SEQ_GDAT register for each of the sequences to e ADC at the end of each ADC conversion. The other is to use these individual ADC Channel Data registers, entire sequence has completed. It is recommended to use one method consistently for a given conversion				
		NOTE				
	The	method to be employed for each sequence should be reflected in the MODE bit in the SEQ_CTRL register e this will impact interrupt and overrun flag generation.				
	The information presented in the DAT registers always pertains to the most recent conversion completed on that channel regardless of what sequence requested the conversion or which trigger caused it.					
	The OVERRUN fi	elds for each channel are also replicated in the FLAGS register.				
	K32W061/K	32W041 Register Manual (Rev. 1.1, 06/2020) at 445-446.				
	15-4	ADC Conversion Result				
	RESULT	This field contains the 12-bit ADC conversion result from the most recent conversion performed under conversion sequence associated with this register. DATAVALID = 1 indicates that this result has not yet been read. If less than 12-bit resolution is used, the ADC result occupies the upper MSBs and unused LSBs should be ignored.				
	K32W061/K See also:	+ 32W041 Register Manual (Rev. 1.1, 06/2020) at 447.				

'474 Patent Claim	Representative NXP Product(s)
	Application sends       Temperature update         to radio driver       Temperature update         vRadio_Tamp.       Temperature update         Update() API       Temperature         T_c       Temperature         Temperature       AOREG1 always on register         Tege 142. Communication between application / MAC SW and Radio SW driver         K32W061/K32W041 User Manual, UM11323 (Rev. 1.1 — June 2020) at 324.
[14a.] A serial communication system comprising:	To the extent the preamble is limiting, the Accused '474 Wireless Microcontrollers include a "serial communication system" as recited in the '474 patent. Exemplary systems and serial interfaces are identified in the block diagrams below. <i>See, e.g.</i> :           See, e.g.:         https://www.nxp.com/docs/en/data-sheet/K32W061.pdf         See also https://www.avnet.com/shop/us/search/k32w041

'474 Patent Claim	Representative NXP Product(s)
	OM15080-K32W (Development Board of K32W061/41)
	https://www.arrow.com/en/products/om15080-k32w/nxp-semiconductors?q=OM15080-K32W



'474 Patent Claim	Representative NXP Product(s)
	1.3 Block diagram         Image: state of the state of
[14b.] a microprocessor having	The Accused '474 Wireless Microcontrollers each includes a microprocessor.
	For example, the Accused '474 Wireless Microcontrollers each constitutes a microprocessor because, among others, they include at the processing logics identified below. <i>See, e.g.</i> :

'474 Patent Claim	Representative NXP Product(s)
	1.3 Block diagram         Image: state
[14c.] a slave serial interface for coupling to a master serial interface through a clock signal line output terminal and a data signal line output terminal	In each of the Accused '474 Wireless Microcontrollers, the microprocessor has a slave serial interface for coupling to a master serial interface through a clock signal line output terminal and a data signal line output terminal. For example, each of the Accused '474 Wireless Microcontrollers has a slave serial interface ( <i>e.g.</i> , I2C) for coupling to a master serial interface ( <i>e.g.</i> , the I2C interface on the master/MCU and/or the host processor) through a clock signal line output terminal ( <i>e.g.</i> , SCL) and a data signal line output terminal



'474 Patent Claim	Representative NXP Product(s)
	25.2 Features
	<ul> <li>Independent Master, Slave, and Monitor functions.</li> <li>Bus speeds supported: <ul> <li>Standard mode, up to 100 kbits/s.</li> <li>Fast-mode, up to 400 kbits/s.</li> <li>Fast-mode Plus, up to 1 Mbits/s (on pins PIO0_10 and PIO0_11 that include</li> </ul> </li> </ul>
	<ul> <li>specific I<sup>2</sup>C support).</li> <li>High speed mode, 3.4 Mbits/s as a Slave only (on pins PIO0_10 and PIO0_11 that include specific I<sup>2</sup>C support).</li> <li>Supports both Multi-master and Multi-master with Slave functions.</li> </ul>
	<ul> <li>Multiple I<sup>2</sup>C slave addresses supported in hardware.</li> <li>One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I<sup>2</sup>C bus addresses.</li> </ul>
	<ul> <li>10-bit addressing supported with software assist.</li> <li>Supports System Management Bus (SMBus).</li> <li>Separate DMA requests for Master, Slave, and Monitor functions.</li> </ul>
	<ul> <li>No chip clocks are required in order to receive and compare an address as a Slave, so this event can wake up the device from deep-sleep mode. Additionally, I<sup>2</sup>C0 can optionally generate a wake-up from power down.</li> </ul>
	<ul> <li>Automatic modes optionally allow less software overhead for some use cases.</li> </ul>
	K32W061/K32W041 User Manual, UM11323 (Rev. 1.1 — June 2020) at 170.



'474 Patent Claim	Representative NXP Product(s)			
	<ul> <li>25.4.2 <sup>12</sup>C receive/transmit in slave mode In this example, <u>PC1 is used as an I<sup>2</sup>C slave.</u> The slave receives 8 bits from the master and then sends 8 bits to the master. The SCL and SDA functions must be enabled on suitable pins, see <u>Table 48</u>. The pins should be configured as required for the I<sup>2</sup>C-bus mode. The transmission of the address and data bits is controlled by the STAT[SLVPENDING] status bit. Whenever the status is Slave pending, the slave can acknowledge ("ack") or send or receive an address and data. The received data or the data to be sent to the master are available in the SLVDAT register. After sending and receiving data, continue to the next step of the transmission protocol by writing to the SLVCTL register.</li> <li>K32W061/K32W041 User Manual, UM11323 (Rev. 1.1 — June 2020) at 173.</li> <li>K32W061/K32W041 User Manual, UM11323 (Rev. 1.1 — June 2020) at 173.</li> </ul>			
[14d.] wherein the slave serial interface is responsive to a read temperature command	In each of the Accused '474 Wireless Microcontrollers, the slave serial interface is responsive to a read temperature command issued by the master serial interface to return to the master serial interface a temperature value associated with the microprocessor.			
issued by the master serial interface to return to the master serial interface a temperature value associated with the microprocessor.	For example, in each of the Accused '474 Wireless Microcontrollers, the slave serial interface ( <i>e.g.</i> , identified above) is responsive to a read temperature command ( <i>e.g.</i> , the read tempearture command requesting the result derived from the temperature sensor measurement) issued by the master serial interface ( <i>e.g.</i> , the factor on the master/MCU and/or the host processor identified above) to return to the master serial interface a temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature value ( <i>e.g.</i> , the result derived from the temperature v			

'474 Patent Claim	Representative NXP Product(s)			
	sensor measurement) associated with the microprocessor identified above.			
	25.4.2.2 Slave write to master			
	This example uses polling to control the sequence and does not use interrupts. Configure the I <sup>2</sup> C as a slave with address x:			
	1. Write the slave address x to the address 0 match register.			
	2. Set the CFG[SLVEN] bit to 1.			
	Write data to the master:			
	<ol> <li>Wait for the pending status to be set (STAT[SLVPENDING] = 1) by polling the STAT register. Check the status register STAT[SLVSTATE] indicating ADDR. If not then an error has occurred.</li> </ol>			
	2. ACK the address by setting SLVCTL[SLVCONTINUE] = 1 in the slave control register.			
	<ol> <li>Wait for the pending status to be set (STAT[SLVPENDING] = 1) by polling the STAT register. Check the status register STAT[SLVSTATE] is indicating TX. If not then an error has occurred.</li> </ol>			
	4. Write 8 bits of data to SLVDAT register.			
	<ol> <li>Continue the transaction by setting SLVCTL[SLVCONTINUE] = 1 in the slave control register.</li> </ol>			

'474 Patent Claim	Representative NXP Product(s)	
	27.2 Features	
	<ul> <li>12-bit successive approximation analog to digital converter.</li> <li>Input multiplexing among up to 8 pins (6 external inputs, 1 temperature sensor and V<sub>BAT</sub>).</li> <li>A configurable conversion sequencer with configurable trigger</li> <li>Optional automatic high/low threshold comparison and "zero crossing" detection.</li> <li>12-bit conversion rate of 190 kHz. Options for reduced resolution at higher conversion rates.</li> <li>Burst conversion mode for single or multiple inputs.</li> <li>Asynchronous operation. Asynchronous mode allows choosing ADC clock from FRO12M or XO32M.</li> <li>A temperature sensor is connected to ADC channel 7, see <u>Chapter 28 "Temperature Sensor"</u> for further details.</li> <li>Supply monitor is connected to ADC channel 6; this monitors V<sub>BAT</sub>.</li> </ul>	
	<ul> <li>Configure the temperature sensor as follows:</li> <li>Select the temperature sensor as source for channel 7 of the ADC by writing the SEQ_CTRL[CHANNELS] bits to 0x80. In order to return ADC channel 7 to measuring its related device pin, write the SEQ_CTRL[CHANNELS] bits to 0x80.</li> <li>The digital temperature reading is available after an analog-to-digital conversion of</li> </ul>	
	ADC channel 7. Remark: To convert the ADC conversion result into a temperature reading, use the API provided. This uses device specific calibration data stored in the device to increase the accuracy of the temperature reading. K32W061/K32W041 User Manual, UM11323 (Rev. 1.1 — June 2020) at 199.	

'474 Patent Claim	Representative NXP Product(s)				
	Table 58. ADC channels				
	ADC channel	Function	Device Pin		
	0	ADC0	PIO14		
	1	ADC1	PIO15		
	2	ADC2	PIO16		
	3	ADC3	PIO17		
	4	ADC4	PIO18		
	5	ADC5	PIO19		
	6	Supply monitor	Internal function		
	7	Temperature sensor	Internal function		
	<u>28.1 How to</u>	UM113 Chapter 28: Rev. 1.1 — Jun o read this chapter	B23 Temperature Sensor ne 2020 Use er nsor is available on all K32W061/41 devices.	er manual	
		The temperature se	isor is available off all K32000 1/41 devices.		
	28.2 Featur	res			
		Linear temperat	ure sensor.		
		<ul> <li>Sensor output in</li> </ul>	nternally connected to the ADC channel 7 for temperature r	nonitoring	
	K32W061/K32	W041 User Manua	al, UM11323 (Rev. 1.1 — June 2020) at	208.	

Basic configuration
This section explains how the Temperature Sensor can be used. For a functional example see lpc_adc_basic.
<ul> <li>Enable the power to the temperature sensor by setting the ASYNC_SYSCON_TEMPSENSORCTRL[ENABLE].</li> </ul>
<ul> <li>Configure temperature sensor common mode output voltage setting ASYNC_SYSCON_TEMPSENSORCTRL[CM] = 0x2 for proper default operation</li> </ul>
<ul> <li>To monitor the temperature continually, select the temperature sensor as source for channel 7 of ADC0. See <u>Chapter 27</u>. The digital temperature reading is available after an analog-to-digital conversion.</li> </ul>
<ul> <li>The ADC reading must be converted into a temperature reading. To increase accuracy the sensor and ADC are calibrated during production, An API is provided to produce a temperature value; this performs the best configuration of the ADC for the purpose of the temperature sensor. The calibration data and other characteristics of the temperature and ADC are used to produce a high accuracy results.</li> </ul>
<ul> <li>For highest accuracy, set ADCCLK mux source to be 32 MHz XTAL with a divider setting of 7, to give an ADCCLK of 4 MHz.</li> </ul>
The voltage range of operation of the ADC is set by ADC_GPADC_CTRL0[TEST]. In normal mode, the ADC can take an input voltage of 0 to 3.6 V, to V <sub>BAT</sub> if this is lower. For the temperature sensor, the ADC must be configured in Unity Gain mode when the input voltage range is 0 to 0.9 V. Since the temperature sensor voltage output is within this range, the best accuracy is achieved. A consequence of this is that the temperature sensor can not be combined with the other ADC inputs as part of sequencer configuration. Also, safe practice is to set the mode back to normal mode after using the ADC with the temperature sensor.
V061/K32W041 User Manual, UM11323 (Rev. 1.1 — June 2020) at 208.
.1 Perform a single ADC conversion with the temperature sensor as ADC input As mentioned in the previous chapter, the API should be used when performing temperature measurements. As a simple example of obtaining a temperature

'474 Patent Claim	Representative NXP Product(s)												
	To perform a single ADC conversion for ADC0 channel 7 using the temperature sensor output:												
	1. Enable the temperature sensor output as input to ADC channel 7.												
	2. Configure the system clock and the ADC for operation.												
	3. Select the asynchronous mode in the ADC_CTRL register.												
	<ol> <li>Select ADC channel 7 to perform the conversion by setting the ADC_SEQ_CTRL[CHANNELS] bits to 0x80.</li> </ol>												
	5. Set the ADC_SEQ_CTRL[START] bit to 1.												
	6. Read the SEQ_GDAT[RESULT] bits for the conversion result.												
	7. The AHI software may be used to generate the temperature value. In fact, the example driver will perform this sequencing as well as making corrections due to the calibration data, and using averaging to give the best result.												
	K32W061/K32W041 User Manual, UM11323 (Rev. 1.1 — June 2020) at 209.												
'474 Patent Claim	Representative NXP Product(s)												
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	17.1.3 ADC Conversion Sequence Control Register (SEQ_CTRL) Offset												
	Register	Offset											
	SEQ_CTRL	8h											
	Function This register controls ADC conversions are or more channels. Diagram	triggering and o	channel selecti ugh this sequer	on for conver ncer which ca	ion sequ be used	ence. Also spe I for a single co	ecifies ir nversio	nterrupt i n or sets	mode for s of conv	r seque ersions	ence. <mark>All</mark> s on one		
	Bits 31 30	29 28	27 26	25 24	23	22 21	20	19	18	17	16		
	W ENA MODE	Reserv SINGL ed ES	BURS T STAR T	STAR T_B		Reserved		SYNC BYP	TRIGP OL	TRIG	GER		
	Reset 0 0	u 0	0 u	0 u	u	u u	u	0	0	0	0		
	Bits 15 14	13 12	11 10	9 8	7	6 5	4	3	2	1	0		
	W TRI	GGER	Res	erved			CHA	NNELS					
	Reset 0 0	0 0	u u	u u	0	0 0	0	0	0	0	0		
	K32W061/K32	W041 Reg	ister Man	ual (Rev	. 1.1,	06/2020)	at 44	0.				_	
	7-0 AE	C Channels											
	CHANNELS Se lau se su eitl ch wh	lect which one inched. A 1 in a quence, where pply monitor. B her by a hardwa annel, in seque ile SEQ_ENA	or more of the any bit of this bit 0 correspo- it 7 is channe are trigger or v nce, beginnin (bit 31) is LOV	e ADC chan field will cau onds to chan I 7; the temp ria software o g with the low V. It is allow	nels will l se the co nel 0, bit erature s ommand est-orde ed to cha	be sampled a prresponding 1 to channel sensor. When d, ADC conve ared channel. I ange this field	nd con channe 1 and this co rsions v Remark and se	verted v el to be i so forth onversio will be p k: This fi et bit 31	when thi included b. Bit 6 is on seque erforme ield can in the s	is sequ d in the s chann ence is d on ea ONLY ame w	ence is convers nel 6; the triggere ach enab be chan rrite.	ilon d, iled ged	

'474 Patent Claim	Representative NXP Product(s)							
	17.1.4 AC	C Sequence Global Data Register (SEQ_GDAT)						
	Register	Offset						
	SEQ_GDAT	10h						
	Function							
	This register conta conversions can b conversion. The o completed. It is rea	ins the result of the most recent ADC conversion completed under each conversion sequence. Results of ADC e read in one of two ways. One is to use this register to read data from the ADC at the end of each ADC ther is to read the individual ADC Channel Data (DATn) registers, typically after the entire sequence has commended to use one method consistently for a given conversion sequence.						
	This register is use sequential (hence address them). Fo retrieve the results	eful in conjunction with DMA operation - particularly when the channels selected for conversion are not the addresses of the individual result registers will not be sequential, making it difficult for the DMA engine to r interrupt-driven code, it will more likely be advantageous to wait for an entire sequence to complete and then s from the individual channel registers.						
		NOTE						
	The r impa	nethod to be employed for each sequence should be reflected in the SEQ_CTRL[MODE] bit since this will ct interrupt and overrun flag generation.						
	K32W061/K	C32W041 Register Manual (Rev. 1.1, 06/2020) at 443.						
	15-4	ADC Conversion Result						
	RESULT	This field contains the 12-bit ADC conversion result from the most recent conversion performed under conversion sequence associated with this register. DATAVALID = 1 indicates that this result has not yet been read. If less than 12-bit resolution is used the ADC result occupies the upper MSBs and unused LSBs should be ignored.						
	K32W061/K	32W041 Register Manual (Rev. 1.1, 06/2020) at 445.						

'474 Patent Claim	Representative NXP Product(s)							
	17.1.5 AD	OC Channel a Data Register (DAT0 - DAT7)						
	Function							
	These registers h when a conversio to the range dicta	old the result of the last conversion completed for each ADC channel. They also include status bits to indicate in has been completed, when a data overrun has occurred, and where the most recent conversion fits relative ted by the high and low threshold registers.						
	Results of ADC or read data from the typically after the sequence.	onversion can be read in one of two ways. One is to use the SEQ_GDAT register for each of the sequences to e ADC at the end of each ADC conversion. The other is to use these individual ADC Channel Data registers, entire sequence has completed. It is recommended to use one method consistently for a given conversion						
		NOTE						
	The	method to be employed for each sequence should be reflected in the MODE bit in the SEQ_CTRL register e this will impact interrupt and overrun flag generation.						
	The information p regardless of what	resented in the DAT registers always pertains to the most recent conversion completed on that channel at sequence requested the conversion or which trigger caused it.						
	The OVERRUN fi	ields for each channel are also replicated in the FLAGS register.						
	K32W061/K	32W041 Register Manual (Rev. 1.1, 06/2020) at 445-446.						
	15-4	ADC Conversion Result						
	RESULT	This field contains the 12-bit ADC conversion result from the most recent conversion performed under conversion sequence associated with this register. DATAVALID = 1 indicates that this result has not yet been read. If less than 12-bit resolution is used, the ADC result occupies the upper MSBs and unused LSBs should be ignored.						
	K32W061/K See also:	+ 32W041 Register Manual (Rev. 1.1, 06/2020) at 447.						



'474 Patent Claim	Representative NXP Product(s)
[1a.] A serial communication system comprising:	To the extent the preamble is limiting, the Accused '474 i.MX Processors include a "serial communication system" as recited in the '474 patent. Exemplary systems and serial interfaces are identified in the block diagrams below.
	See, e.g., :
	https://www.avnet.com/shop/us/products/nxp/mcimx6d6avt08ac-3074457345639626703/



'474 Patent Claim	Representative NXP Product(s)
	WIMAGGAVT10AD Development Board (Mouser)
	WCIMX6DP6AVT8AA (Mouser)





'474 Patent Claim	Representative NXP Product(s)							
	System Control Secure JTAG	CPU Platform	Conne MMC 4.4/	USB2 HSIC				
	PLL, Osc.	32 KB I-Cache 32 KB D-Cache per Core per Core	SD 3.0 x3	Host x2				
	Smart DMA	NEON per Core PTM per Core	SDXC	S/PDIF				
	IOMUX	1 MB L2-Cache + VFPv3 Multimedia	5 Mbps	PCIe 2.0				
	Timer x3 PWM x4	Hardware Graphics Accelerators 3D Vector Graphics	IFC x3, SPI x5	(1-Lane)				
	Watch Dog x2	2D	ESAI, I <sup>I</sup> S/SSI x3	MLB150 + DTCP				
	Power Management Power Supplies Monitor	1080p30 Enc/Dec ASRC	3.3V GPIO	1 Gb Ethemet + IEEE® 1588				
	Internal Memory ROM RAM	Resizing and Blending Image Enhancement Inversion/Rotation	S-ATA and PHY 3 Gbps	NAND Cntrl. (BCH40)				
	Security           RNG         Security Critri           TrustZone         Secure RTC           Ciphers         sFuses	Display and Camera Interface           HDMI and PHY         24-bit RGB, LVDS (x2)           MIPI DSI         20-bit CSI           MIPI CSI2         20-bit CSI	USB2 OTG and PHY USB2 Host and PHY	LP-DDR2, DDR3/ LV-DDR3 x32/64, 533 MHz				
	https://www.nxp.com/ processors/i-mx-6-proc cortex-a9-core:i.MX60	products/processors-and-microco cessors/i-mx-6quad-processors-h Q	ontrollers/arr igh-perform	n-processor ance-3d-gra	s/i-mx-applications- phics-hd-video-arm-			
[1b.] an integrated circuit having a master serial interface; and	The Accused '474 i.M For example, the Accu serial interface ( <i>e.g.</i> , th <i>See, e.g.</i> :	X Processors each includes an in used '474 i.MX Processors each i ne I2C interface on the master/M4	tegrated circ ncludes an in CU and/or th	cuit having a ntegrated ci ne host proc	a master serial interface. rcuit having a master essor).			





'474 Patent Claim	Representative NXP Product(s)								
	System Control Secure JTAG	CPU Platform CPU Platform MMC 4.4/ USB2 HSIC							
	PLL, Osc. Clock and Reset Smart DMA	32 KB I-Cache per Core     32 KB D-Cache per Core     SD 3.0 x3     Host x2       NEON per Core     PTM per Core     MMC 4.4/ SDXC     MIPI HSI							
	IOMUX Timer x3 PWM x4	1 MB L2-Cache + VFPv3     5 Mbps     1x/hx       Multimedia     FC x3, SPI x5     PCle 2.0 (1-Lane)							
	Watch Dog x2	2D ESAI, PS/SSI X3 DTCP							
	Power Management Power Temperature	Video Codecs Audio 1080p30 Enc/Dec ASRC 3.3V GPIO 1 Gb Ethemet + IEEE* 1588							
	Internal Memory ROM RAM	Imaging Processing Unit         Keypad           Resizing and Blending Image Enhancement         S-ATA and PHY 3 Gbps         NAND Cntrl. (BCH40)							
	Security RNG Security Critity TrustZone Secure RTC Ciphers eFuses https://www.nxp.com/processors/i-mx-6-processors/i	Display and Camera Interface       USB2 OTG         HDMI and PHY       24-bit RGB, LVDS (x2)         MIPI DSI       20-bit CSI         MIPI CSI2       USB2 Host         /products/processors-and-microcontrollers/arm-processors/i-mx-applications-         cessors/i-mx-6quad-processors-high-performance-3d-graphics-hd-video-arm-							
	cortex-a9-core:i.MX60	Q							

'474 Patent Claim	Representative NXP Product(s)						
	Chapter 35 I2C Controller (I2C)						
	35.1 Overview						
	This chapter describes block-level operation and programming of I2C. The chapter is intended for a block-driver software developer. To understand how the block is integrated at the SoC level, a system software developer should see discussions of the block in the appropriate SoC-level chapter(s).						
	References: This document assumes an understanding of the following document:						
	The I2C Bus Specification, Version 2.1, by Philips Semiconductor						
	The Inter IC (I2C) provides functionality of a standard I2C slave and master. The I2C is designed to be compatible with the standard NXP I2C bus protocol.						
	NOTE Three independent I2C channels are available.						
	I2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I2C standard allows additional devices to be connected to the bus for expansion and system development. See the connection diagram in the figure below.						
	i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: IMX6DQRM (Rev 2, 06/2014) at 1893.						



'474 Patent Claim	Representative NXP Product(s)	
	<b>35.4.1 I2C system configuration</b> After a reset, the I2C defaults to Slave Receive operations. Thus, when not operating as a master or responding to a slave transmit address, the I2C defaults to the Slave Receive state.	
	i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: IM 2, 06/2014) at 1897.	1X6DQRM (Rev
	<b>NOTE</b> The I2C is designed to be compatible with the Philips <sup>TM</sup> I2C bus protocol. For information on system configuration, protocol, and restrictions, see the <i>I2C Bus Specification</i> , version 2.1, by Philips Semiconductors. The I2C supports Standard and Fast modes only.	
	i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: IM 2, 06/2014) at 1898.	1X6DQRM (Rev

'474 Patent Claim	Representative NXP Product(s)											
	35.7.3 I The I2C_I2 govern ope	2C Co CR is us ration as	ntrol Re sed to enal a slave or	egister ( ble the I2C a master.	I2Cx_I2 and the I	<b>CR)</b> 2C interru	pt. It also	contains b	its that			
	Address. base a	15	14	13	12	11	10	9	8			
	Read				Ĵ	D						
	Write											
	Reset	0	0	0	0	0	0	0	0			
	Bit	7	6	5	4	3	2	1	0			
	Read	IEN	IIEN	MSTA	MTX	тхак	0 BSTA	(	D:			
	Reset	0	0	0	0	0	0	0	0			
	i.MX 6Dual 2, 06/2014) 35.7.4 The I2C_ i.MX 6Dual	/6Quad at 1913 <b>I2C S</b> I2SR co /6Quad	Applica tatus F ntains bit	Actions Pro Register as that ind	• (I2Cx_ icate tran	Reference [ <b>12SR</b> ] saction di Reference	rection ar	al, Docu nd status. al, Docu	ment Nu	umber: IN	AX6DQR AX6DQR	2M (Rev 2M (Rev
	2, 06/2014)	at 1914			0003501			ui, Doou				

'474 Patent Claim	Representative NXP Product(s)	
	35.7.5 I2C Data I/O Register (I2Cx_I2DR)	
	In Master Receive mode, reading the data register allows a read to occur and initiates the next byte to be received. In Slave mode, the same function is available after it is addressed.	
	i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: I 2, 06/2014) at 1916.	MX6DQRM (Rev
[1c.] a processor having a slave serial interface coupled to the master serial	The Accused '474 i.MX Processors each includes a processor having a slave serial in the master serial interface through a clock signal line and a data signal line.	terface coupled to
interface through a clock signal line and a data signal line	For example, the Accused '474 i.MX Processors each includes a processor having a sinterface ( <i>e.g.</i> , the I2C interface on the slave processor) coupled to the master serial is above through a clock signal line ( <i>e.g.</i> , SCL) and a data signal line ( <i>e.g.</i> , SDA).	slave serial nterface identified

'474 Patent Claim	Representative NXP Product(s)						
	Chapter 35 I2C Controller (I2C)						
	35.1 Overview						
	This chapter describes block-level operation and programming of I2C. The chapter is intended for a block-driver software developer. To understand how the block is integrated at the SoC level, a system software developer should see discussions of the block in the appropriate SoC-level chapter(s).						
	References: This document assumes an understanding of the following document:						
	The I2C Bus Specification, Version 2.1, by Philips Semiconductor						
	The Inter IC (I2C) provides functionality of a standard I2C slave and master. The I2C is designed to be compatible with the standard NXP I2C bus protocol.						
	NOTE Three independent I2C channels are available.						
	I2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I2C standard allows additional devices to be connected to the bus for expansion and system development. See the connection diagram in the figure below.						
	i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: IMX6DQRM (Rev 2, 06/2014) at 1893.						



'474 Patent Claim	Representative NXP Product(s)				
	<b>35.4.1 I2C system configuration</b> After a reset, the I2C defaults to Slave Receive operations. Thus, when not operating as a master or responding to a slave transmit address, the I2C defaults to the Slave Receive state.				
	i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: IM 2, 06/2014) at 1897.	1X6DQRM (Rev			
	<b>NOTE</b> The I2C is designed to be compatible with the Philips <sup>TM</sup> I2C bus protocol. For information on system configuration, protocol, and restrictions, see the <i>I2C Bus Specification</i> , version 2.1, by Philips Semiconductors. The I2C supports Standard and Fast modes only.				
	i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: IM 2, 06/2014) at 1898.	1X6DQRM (Rev			

'474 Patent Claim					Represe	entative	NXP Pro	oduct(s)				
	35.7.3 I The I2C_I2 govern ope	2C Co CR is us ration as	ntrol Re sed to enal a slave or	egister ( ble the I2C a master.	I2Cx_I2	<b>CR)</b> 2C interru	pt. It also	contains b	its that			
	Address. base a	15	14	13	12	11	10	9	8			
	Read					D						
	Write											
	Reset	0	0	0	0	0	0	0	0			
	Bit	7	6	5	4	3	2	1	0			
	Read	IEN	IIEN	MSTA	MTX	ТХАК	0	(	)			
	Write	0	0	0	0	0	RSTA	0	0			
	Reset	U	U	U	U	U	U	0	0			
	i.MX 6Dual 2, 06/2014) 35.7.4 The I2C_	6Quad at 1913 <b>12C S</b> 12SR co	Applica tatus F	egister	• (I2Cx_ icate tran	Reference [12SR] saction di	irection ar	al, Docu	ment Nu		1X6DQR	M (Rev
	i.MX 6Dual 2, 06/2014)	/6Quad at 1914	Applica	tions Pro	ocessor	Referen	ce Manu	al, Docu	ment Nu	imber: IN	/IX6DQR	M (Rev

'474 Patent Claim	Representative NXP Product(s)						
	35.7.5 I2C Data I/O Register (I2Cx_I2DR)						
	In Master Receive mode, reading the data register allows a read to occur and initiates the next byte to be received. In Slave mode, the same function is available after it is addressed. i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: IMX6DORM (Rev						
	2, 06/2014) at 1916.						
	Address: Base address + 10h offset           Bit         15         14         13         12         11         10         9         8         7         6         5         4         3         2         1         0           DATA						
	Reset         0						
	Field         Description           15-8         This read-only field is reserved and always has the value 0.           Reserved         Reserved						
	DATA Data Byte. Holds the last data byte received or the next data byte to be transferred. Software writes the next data byte to be transmitted or reads the data byte received.  NOTE: The core-written value in I2C_I2DR cannot be read back by the core. Only data written by the I2C bus side can be read.						
	i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: IMX6DQRM (Rev 2, 06/2014) at 1916.						
[1d.] wherein the slave serial interface is responsive to a read temperature command	In each of the Accused '474 i.MX Processors, the slave serial interface is responsive to a read temperature command issued by the master serial interface to return a temperature value associated with the processor.						
issued by the master serial interface to return a temperature value associated with the	For example, in each of the Accused '474 i.MX Processors, the slave serial interface identified above is responsive to a read temperature command ( <i>e.g.</i> , the read tempearture command requesting the result derived from the temperature monitor "TEMPMON" measurement) issued by the identified master						

'474 Patent Claim	Representative NXP Product(s)					
processor.	serial interface to return a temperature value ( <i>e.g.</i> , the result derived from the temperature monitor "TEMPMON" measurement) associated with the processor.					
	35.7.5 I2C Data I/O Register (I2Cx_I2DR)					
	In Master Receive mode, reading the data register allows a read to occur and initiates the next byte to be received. In Slave mode, the same function is available after it is addressed.					
	i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: IMX6DQRM (Rev 2, 06/2014) at 1916.					
	Read 0 DATA					
	Reset         0					
	Field Description					
	15–8 This read-only field is reserved and always has the value 0. Reserved					
	DATA Data Byte. Holds the last data byte received or the next data byte to be transferred. Software writes the next data byte to be transmitted or reads the data byte received.  NOTE: The core-written value in I2C_I2DR cannot be read back by the core. Only data written by the I2C bus side can be read.					
	i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: IMX6DQRM (Rev 2, 06/2014) at 1916.					

'474 Patent Claim	Representative NXP Product(s)					
	10.4.2.2 Thermal-aware power management					
	The temperature sensor block (TEMPMON) implements a temperature sensor/conversion function. The block features an alarm function that can raise an interrupt signal if the temperature is above a specified threshold.					
	Software may implement temperature aware DVFS for the ARM domain and the GPU domain, as well as temperature aware frequency scaling for other system components to ensure that both the frequency and voltage is lowered when the die temperature is above the specified limit.					
	Software may also implement temperature aware task scheduling to ensure that non- critical tasks are suspended when the die temperature is above the specified limit.					
	See Temperature Monitor (TEMPMON) for further details on temperature monitor functions and programmability options.					
	Chapter 62 Temperature Monitor (TEMPMON)					
	The temperature sensor module implements a temperature sensor/conversion function					
	based on a temperature-dependent voltage to time conversion.					
	is above a specified threshold. A self-repeating mode can also be programmed which executes a temperature sensing operation based on a programmed delay.					
	Software can use this module to monitor the on-die temperature and take appropriate actions such as throttling back the core frequency when a temperature interrupt is set.					
	The high-level implementation of the temperature sensor is shown in the figure below.					
	i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: IMX6DQRM (Rev					



'474 Patent Claim	Representative NXP Product(s)					
		TEMPMON_TEMPSENSE0n field descriptions				
	Field	Description				
	31-20 ALARM_VALUE	This bit field contains the temperature count (raw sensor output) that will generate an alarm interrupt.				
	19-8 TEMP_CNT	This bit field contains the last measured temperature count.				
	7	This field is reserved. Reserved.				
	6	This field is reserved. Reserved.				
	5-3	This field is reserved. Reserved				
	2 FINISHED	Indicates that the latest temp is valid. This bit should be cleared by the sensor after the start of each measurement.				
		1 VALID — Last measurement is valid.				
	1 MEASURE_	Starts the measurement process. If the measurement frequency is zero in the TEMPSENSE1 register, this results in a single conversion.				
	i.MX 6Dual/6Q 2, 06/2014) at 5	uad Applications Processor Reference Manual, Document Number: IMX6DQRM (Rev 163.				
	The Accused '4 temperature cor	74 i.MX Processors reads and returns the "TEMPMON" value in response to a read nmand issued by an external I2C master.				
	See, e.g.:					

'474 Patent Claim	Representative NXP Product(s)	
	<pre>if (status &amp; I2SR_SRW) { /* Master wants to read from us*/     dev_dbg(&amp;i2c_imx-&gt;adapter.dev, "read requested");     i2c_slave_event(i2c_imx-&gt;slave, I2C_SLAVE_READ_REQUESTED, &amp;value);</pre>	
	/* Slave transmit */ ctl  = I2CR_MTX; imx_i2c_write_reg(ctl, i2c_imx, IMX_I2C_I2CR);	
	<pre>/* Send data */ imx_i2c_write_reg(value, i2c_imx, IMX_I2C_I2DR); } else { /* Master wants to write to us */     dev_dbg(&amp;i2c_imx-&gt;adapter.dev, "write requested");     i2c_slave_event(i2c_imx-&gt;slave, I2C_SLAVE_WRITE_REQUESTED, &amp;value);</pre>	
	https://patchwork.kernel.org/project/linux-arm-kernel/patch/20191009101802.19309-1- biwen.li@nxp.com/	
[8a.]. A method for communicating over a point to point serial communication system	To the extent the preamble is limiting, the Accused '474 i.MX Processors perform a method for communicating over a point to point serial communication system having a clock signal line and a signal line coupling a serial interface master and a serial interface slave.	ı data
having a clock signal line and a data signal line coupling a serial interface master and a serial interface slave, the method comprising:	For example, each of the Accused '474 i.MX Processors perform a method for communicating over point to point serial communication system identified below having a clock signal line ( <i>e.g.</i> , SCL) data signal line ( <i>e.g.</i> , SDA) coupling a serial interface master ( <i>e.g.</i> , the I2C interface on the master/MCU and/or the host processor) and a serial interface slave ( <i>e.g.</i> , the I2C interface on the sprocessor).	er a and a lave
	See, e.g.:	

'474 Patent Claim	Representative NXP Product(s)
	https://www.avnet.com/shop/us/products/nxp/mcimx6d6avt08ac-3074457345639626703/



'474 Patent Claim	Representative NXP Product(s)
	WIMKeQeAVT10AD Development Board (Mouser)
	WCIMX6DP6AVT8AA (Mouser)





'474 Patent Claim	Representative NXP Product(s)				
	System Control Secure JTAG	CPU Platform	Conne MMC 4.4/	ctivity USB2 HSIC	
PLL, Osc. Clock and Reset Smart DMA	Quad ARM* Cortex***-A9 Core       32 KB I-Cache per Core       32 KB I-Cache per Core       NEON per Core       PTM per Core	SD 3.0 x3 MMC 4.4/ SDXC	Host x2 MIPI HSI S/PDIF		
	IOMUX Timer x3	1 MB L2-Cache + VFPv3 Multimedia Hardware Graphics Accelerators	UART x5, 5 Mbps FC x3, SPI x5	Tx/Rx PCle 2.0 (1-Lane)	
	PWM x4 Watch Dog x2 Power Management	3D Vector Graphics 2D Video Codecs Audio	ESAI, I <sup>I</sup> S/SSI x3	FlexCAN x2 MLB150 + DTCP	
	Power Supplies Temperature Monitor	1080p30 Enc/Dec ASRC	3.3V GPIO Keypad	1 Gb Ethemet + IEEE* 1588	
	ROM RAM Security RNG Security Criter	Inversion/Rotation Display and Camera Interface	S-ATA and PHY 3 Gbps	(BCH40)	
	TrustZone Secure RTC Giphers eFuses	HDMI and PHY 24-bit RGB, LVDS (x2) MIPI DSI 20-bit CSI MIPI CSI2	and PHY USB2 Host and PHY	LV-DDR3 x32/64, 533 MHz	
	https://www.nxp.com/ processors/i-mx-6-proc cortex-a9-core:i.MX60	products/processors-and-microcon cessors/i-mx-6quad-processors-hig 2	trollers/arm h-performa	n-processors/i-mx-applications- ance-3d-graphics-hd-video-arm-	

'474 Patent Claim	Representative NXP Product(s)
	Chapter 35 I2C Controller (I2C)
	35.1 Overview
	This chapter describes block-level operation and programming of I2C. The chapter is intended for a block-driver software developer. To understand how the block is integrated at the SoC level, a system software developer should see discussions of the block in the appropriate SoC-level chapter(s).
	References: This document assumes an understanding of the following document:
	• The I2C Bus Specification, Version 2.1, by Philips Semiconductor
	The Inter IC (I2C) provides functionality of a standard I2C slave and master. The I2C is designed to be compatible with the standard NXP I2C bus protocol.
	NOTE Three independent I2C channels are available.
	I2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I2C standard allows additional devices to be connected to the bus for expansion and system development. See the connection diagram in the figure below.
	i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: IMX6DQRM (Rev 2, 06/2014) at 1893.


'474 Patent Claim	Representative NXP Product(s)	
	<b>35.4.1 I2C system configuration</b> After a reset, the I2C defaults to Slave Receive operations. Thus, when not operating as a master or responding to a slave transmit address, the I2C defaults to the Slave Receive state.	
	i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: IM 2, 06/2014) at 1897.	1X6DQRM (Rev
	<b>NOTE</b> The I2C is designed to be compatible with the Philips <sup>TM</sup> I2C bus protocol. For information on system configuration, protocol, and restrictions, see the <i>I2C Bus Specification</i> , version 2.1, by Philips Semiconductors. The I2C supports Standard and Fast modes only.	
	i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: IM 2, 06/2014) at 1898.	1X6DQRM (Rev

'474 Patent Claim	Representative NXP Product(s)											
	35.7.3 I The I2C_I2 govern ope	2C Col	ntrol Re ed to enal a slave or	egister ( ble the I2C a master.	and the I	<b>CR)</b> 2C interru	pt. It also	contains b	its that			
	Address. base a	15	14	13	12	11	10	9	8			
	Read					0						
	Write					0						
	Reset	0	0	0	0	0	0	0	0			
	Bit	7	6	5	4	3	2	1	0			
	Head	IEN	IIEN	MSTA	MTX	ТХАК	U		J			
	Reset	0	0	0	0	0	0	0	0			
	i.MX 6Dual 2, 06/2014) 35.7.4 The I2C_ i.MX 6Dual	/6Quad at 1913 <b>I2C S</b> I2SR co /6Quad	Applica tatus F ntains bit Applica	ations Pro legister s that ind	• (I2Cx_ icate tran	Reference [ <b>12SR</b> ] saction di Reference	ce Manua irection ar ce Manua	al, Docu nd status. al, Docu	ment Nu	umber: IN	4X6DQF MX6DQF	RM (Rev
	2, 06/2014)	at 1914						,			- (-	× ·

'474 Patent Claim	Representative NXP Product(s)										
	35.7.5 I2C Data I/O Register (I2Cx_I2DR) In Master Receive mode, reading the data register allows a read to occur and initiates the										
	i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: IMX6DQRM (Rev 2, 06/2014) at 1916.										
	Address: Base address + 10h offset       Bit     15     14     13     12     11     10     9     8     7     6     5     4     3     2     1     0       Read     0     DATA										
	Write         Reset         0										
	I2Cx_I2DR field descriptions										
	Field Description										
	15-8 This read-only field is reserved and always has the value 0. Reserved										
	DATA Data Byte. Holds the last data byte received or the next data byte to be transferred. Software writes the next data byte to be transmitted or reads the data byte received. NOTE: The core-written value in I2C_I2DR cannot be read back by the core. Only data written by the I2C bus side can be read.										
	i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: IMX6DQRM (Rev 2, 06/2014) at 1916.										
[8b.] sending a read temperature command to the serial interface slave	The Accused '474 i.MX Processors performs a step of sending a read temperature command to the serial interface slave from the serial interface master using the clock signal line and the data signal line.										
from the serial interface	For example, each of the Accused '474 i.MX Processors perform a step of sending a read temperature										
master using the clock	command ( <i>e.g.</i> , the read tempearture command requesting the result derived from the temperature										
signal line and the data	interface master identified above using the clock signal line identified above and the data signal line										
signal line; and	identified above using the clock signal line identified above and the data signal line										

'474 Patent Claim	Representative NXP Product(s)								
	See, e.g.,								
	35.7.5 I2C Data I/O Register (I2Cx_I2DR)								
	In Master Receive mode, reading the data register allows a read to occur and initiates the next byte to be received. In Slave mode, the same function is available after it is addressed.								
	i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: IMX6DQRM (Rev 2, 06/2014) at 1916.								
	Address: Base address + 10h offset           Bit         15         14         13         12         11         10         9         8         7         6         5         4         3         2         1         0           DATA								
	Write Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0								
	I2Cx_I2DR field descriptions								
	Field Description								
	15-8 This read-only field is reserved and always has the value 0. Reserved								
	DATA Data Byte. Holds the last data byte received or the next data byte to be transferred. Software writes the next data byte to be transmitted or reads the data byte received. NOTE: The core-written value in I2C_I2DR cannot be read back by the core. Only data written by the I2C bus side can be read.								
	i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: IMX6DQRM (Rev 2, 06/2014) at 1916.								

'474 Patent Claim	Representative NXP Product(s)
	10.4.2.2 Thermal-aware power management
	The temperature sensor block (TEMPMON) implements a temperature sensor/conversion function. The block features an alarm function that can raise an interrupt signal if the temperature is above a specified threshold.
	Software may implement temperature aware DVFS for the ARM domain and the GPU domain, as well as temperature aware frequency scaling for other system components to ensure that both the frequency and voltage is lowered when the die temperature is above the specified limit.
	Software may also implement temperature aware task scheduling to ensure that non- critical tasks are suspended when the die temperature is above the specified limit.
	See Temperature Monitor (TEMPMON) for further details on temperature monitor functions and programmability options.
	Chapter 62 Temperature Monitor (TEMPMON)
	The temperature sensor module implements a temperature sensor/conversion function
	based on a temperature-dependent voltage to time conversion.
	The module features an alarm function that can raise an interrupt signal if the temperature is above a specified threshold. A self-repeating mode can also be programmed which executes a temperature sensing operation based on a programmed delay.
	Software can use this module to monitor the on-die temperature and take appropriate actions such as throttling back the core frequency when a temperature interrupt is set.
	The high-level implementation of the temperature sensor is shown in the figure below.
	i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: IMX6DQRM (Rev



'474 Patent Claim	Representative NXP Product(s)							
		TEMPMON_TEMPSENSE0n field descriptions						
	Field	Description						
	31-20 ALARM_VALUE	This bit field contains the temperature count (raw sensor output) that will generate an alarm interrupt.						
	19-8 TEMP_CNT	This bit field contains the last measured temperature count.						
	7	This field is reserved. Reserved.						
	6	This field is reserved. Reserved.						
	53 -	This field is reserved. Reserved						
	2 FINISHED	Indicates that the latest temp is valid. This bit should be cleared by the sensor after the start of each measurement.						
		INVALID — Last measurement is not ready yet.     VALID — Last measurement is valid.						
	1 MEASURE_ TEMP	Starts the measurement process. If the measurement frequency is zero in the TEMPSENSE1 register, this results in a single conversion.						
	i.MX 6Dual/6Q 2, 06/2014) at 5	uad Applications Processor Reference Manual, Document Number: IMX6DQRM (Rev 163.						
	The Accused '4 temperature cor	74 i.MX Processors reads and returns the "TEMPMON" value in response to a read nmand issued by an external I2C master.						
	See, e.g.:							

'474 Patent Claim	Representative NXP Product(s)
	<pre>if (status &amp; I2SR_SRW) { /* Master wants to read from us*/     dev_dbg(&amp;i2c_imx-&gt;adapter.dev, "read requested");     i2c_slave_event(i2c_imx-&gt;slave, I2C_SLAVE_READ_REQUESTED, &amp;value);</pre>
	/* Slave transmit */ ctl  = I2CR_MTX; imx_i2c_write_reg(ctl, i2c_imx, IMX_I2C_I2CR);
	<pre>/* Send data */ imx_i2c_write_reg(value, i2c_imx, IMX_I2C_I2DR); } else { /* Master wants to write to us */     dev_dbg(&amp;i2c_imx-&gt;adapter.dev, "write requested");     i2c_slave_event(i2c_imx-&gt;slave, I2C_SLAVE_WRITE_REQUESTED, &amp;value);</pre>
	https://patchwork.kernel.org/project/linux-arm-kernel/patch/20191009101802.19309-1- biwen.li@nxp.com/
[8c.] in response to the read temperature command, the serial interface slave	The Accused '474 i.MX Processors performs a step of in response to the read temperature command, the serial interface slave supplying over the data signal line a temperature value associated with a processor on an integrated circuit containing the serial interface slave.
signal line a temperature value associated with a processor on an integrated circuit containing the serial interface slave.	For example, each of the Accused '474 i.MX Processors perform a step of in response to the read temperature command, the serial interface slave identified above supplying over the data signal line identified above a temperature value ( <i>e.g.</i> , the result derived from the temperature monitor "TEMPMON" measurement) associated with a processor on an integrated circuit containing the serial interface slave identified above.
	See, e.g.,

'474 Patent Claim		Representative NXP Product(s)																
	35.7.5	I2C D	ata I/O	Regist	er (l:	2Cx	l2D	R)										_
	In Master Receive mode, reading the data register allows a read to occur and initiates the next byte to be received. In Slave mode, the same function is available after it is addressed.							(Rev										
	2, 06/2014	at 1916	).		00000	501 1.		nie e	141411	.uui,	DUC	unier	it i vanio	01.11	11102	Q10.1	(100)	
	Address: Base a Bit 15 Read	ddress + 10h 14 13	offset 12 11 0	10 9	8	7	6	5	4	3	2	1	0					
	Write						1270	1.25	DAI	A	14211	2						
	Reset 0	0 0	0 0	0 0	0	0	0	0	0	0	0	0	0					
	1		1	2Cx_I2DR	field	descri	ptions	s										
	Field					Descrip	otion											
	15–8 Reserved	This read-	only field is re	served and alw	ays has	the valu	Je 0.											
	DATA	Data Byte. next data	Holds the las	t data byte reci smitted or rea/	eived or Is the di	the next ata byte	t data by received	/te to be J.	) transfe	rred. So	oftware	writes th	he					
		NOTE: T	he core-writter us side can be	n value in I2C_ e read.	I2DR ca	innot be	read ba	ick by th	ie core.	Only da	ata writte	en by the	e 12C					
	i.MX 6Du	.1/6Ouac	Applic	ations Pr	oces	sor R	efere	ence	Man	ual.	Doc	umer	 nt Numb	er: IN	AX6D	ORM	(Rev	
	2. 06/2014	at 1916	).							,						<b>X</b>	(	
	_, _ ,		-															
	1																	

'474 Patent Claim	Representative NXP Product(s)
	10.4.2.2 Thermal-aware power management
	The temperature sensor block (TEMPMON) implements a temperature sensor/conversion function. The block features an alarm function that can raise an interrupt signal if the temperature is above a specified threshold.
	Software may implement temperature aware DVFS for the ARM domain and the GPU domain, as well as temperature aware frequency scaling for other system components to ensure that both the frequency and voltage is lowered when the die temperature is above the specified limit.
	Software may also implement temperature aware task scheduling to ensure that non- critical tasks are suspended when the die temperature is above the specified limit.
	See Temperature Monitor (TEMPMON) for further details on temperature monitor functions and programmability options.
	Chapter 62 Temperature Monitor (TEMPMON)
	62.1 Overview
	based on a temperature-dependent voltage to time conversion.
	The module features an alarm function that can raise an interrupt signal if the temperature is above a specified threshold. A self-repeating mode can also be programmed which executes a temperature sensing operation based on a programmed delay.
	Software can use this module to monitor the on-die temperature and take appropriate actions such as throttling back the core frequency when a temperature interrupt is set.
	The high-level implementation of the temperature sensor is shown in the figure below.
	i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: IMX6DQRM (Rev



'474 Patent Claim	Representative NXP Product(s)							
		TEMPMON_TEMPSENSE0n field descriptions						
	Field	Description						
	31-20 ALARM_VALUE	This bit field contains the temperature count (raw sensor output) that will generate an alarm interrupt.						
	19-8 TEMP_CNT	This bit field contains the last measured temperature count.						
	7	This field is reserved. Reserved.						
	6	This field is reserved. Reserved.						
	53 -	This field is reserved. Reserved						
	2 FINISHED	Indicates that the latest temp is valid. This bit should be cleared by the sensor after the start of each measurement.						
		INVALID — Last measurement is not ready yet.     VALID — Last measurement is valid.						
	1 MEASURE_ TEMP	Starts the measurement process. If the measurement frequency is zero in the TEMPSENSE1 register, this results in a single conversion.						
	i.MX 6Dual/6Q 2, 06/2014) at 5	uad Applications Processor Reference Manual, Document Number: IMX6DQRM (Rev 163.						
	The Accused '4 temperature cor	74 i.MX Processors reads and returns the "TEMPMON" value in response to a read nmand issued by an external I2C master.						
	See, e.g.:							

'474 Patent Claim	Representative NXP Product(s)
	<pre>if (status &amp; I2SR_SRW) { /* Master wants to read from us*/     dev_dbg(&amp;i2c_imx-&gt;adapter.dev, "read requested");     i2c_slave_event(i2c_imx-&gt;slave, I2C_SLAVE_READ_REQUESTED, &amp;value);     /* Slave transmit */     ctl  = I2CR_MTX;     imx_i2c_write_reg(ctl, i2c_imx, IMX_I2C_I2CR);     /* Send data */     imx_i2c_write_reg(value, i2c_imx, IMX_I2C_I2DR); } else { /* Master wants to write to us */     dev_dbg(&amp;i2c_imx-&gt;adapter.dev, "write requested");     i2c_slave_event(i2c_imx-&gt;slave, I2C_SLAVE_WRITE_REQUESTED, &amp;value);  https://patchwork.kernel.org/project/linux-arm-kernel/patch/20191009101802.19309-1- </pre>
[14a.] A serial communication system	To the extent the preamble is limiting, the Accused '474 i.MX Processors include a "serial communication system" as recited in the '474 patent. Exemplary systems and serial interfaces are identified in the block diagrams below.
comprising.	See, e.g.:

'474 Patent Claim	Representative NXP Product(s)
	https://www.avnet.com/shop/us/products/nxp/mcimx6d6avt08ac-3074457345639626703/



'474 Patent Claim	Representative NXP Product(s)
	WIMKeQeAVT10AD Development Board (Mouser)
	WCIMX6DP6AVT8AA (Mouser)





'474 Patent Claim		Representative	NXP Pro	duct(s)	
	System Control		Conne	ctivity	
	Secure JTAG PLL, Osc.	CPU Platform Quad ARM® Cortex™-A9 Core 32 KB I-Cache 32 KB D-Cache	MMC 4.4/ SD 3.0 x3	USB2 HSIC Host x2	
	Clock and Reset	per Core per Core	MMC 4.4/ SDXC	MIPI HSI	
	Smart DMA	1 MB L2-Cache + VFPv3	UART x5, 5 Mbps	S/PDIF Tx/Rx	
	Timer x3	Multimedia Hardware Graphics Accelerators	FC x3, SPI x5	PCIe 2.0 (1-Lane)	
	Watch Dog x2	2D Vector Graphics	ESAI, I <sup>s</sup> S/SSI	FlexCAN x2 MLB150 + DTCP	
	Power Management Power Temperature Supplies Monitor	Video Codecs Audio 1080p30 Enc/Dec ASRC	3.3V GPIO	1 Gb Ethemet + IEEE® 1588	
	Internal Memory	Imaging Processing Unit Resizing and Blending Image Enhancement	Keypad	NAND Cntrl.	
	ROM RAM	Inversion/Rotation	S-ATA and PHY 3 Gbps	(BCH40)	
	RNG         Security Cntil,           TrustZone         Secure RTC           Ciptiers         eFuses	Display and Camera Interface       HDMI and PHY     24-bit RGB, LVDS (x2)       MIPI DSI     20-bit CSI       MIPI CSI2     20-bit CSI	USB2 OTG and PHY USB2 Host and PHY	LP-DDR2, DDR3/ LV-DDR3 x32/64, 533 MHz	
	https://www.nxp.com/ processors/i-mx-6-proces	/products/processors-and-mic ocessors/i-mx-6quad-processo Q	erocontroll prs-high-pe	ers/arm-pro erformance	ocessors/i-mx-applications- -3d-graphics-hd-video-arm-
[14b.] a microprocessor having	The Accused '474 i.M	IX Processors each includes a	a micropro	cessor.	
	For example, the Accurate others, they include at	used '474 i.MX Processors ea the processing logics identif	ach constit ied below.	utes a micr	oprocessor because, among
	See, e.g.:				





'474 Patent Claim		Representative NX	P Product(s)	)	
	System Control Secure JTAG	CPU Platform	Conne MMC 4.4/	USB2 HSIC	
	PLL, Osc.	32 KB I-Cache 32 KB D-Cache	SD 3.0 x3 MMC 4.4/ SDXC	Host x2	
	Clock and Reset	per Core per Core		MIPI HSI	
	Smart DMA	NEON per core P1M per core		S/PDIF	
	IOMUX	1 MB L2-Cache + VFPv3	5 Mbps	PCIa 2.0	
	Timer x3 PWM x4	Multimedia Hardware Graphics Accelerators	IFC x3, SPI x5	(1-Lane)	
	Watch Dog x2	2D Vector Graphics	ESAI, I <sup>I</sup> S/SSI x3	FlexCAN x2 MLB150 + DTCP	
	Power Management Power Supplies Temperature Monitor Internal Memory ROM RAM	Video Codecs Audio 1080p30 Enc/Dec ASRC	3.3V GPIO Keypad S-ATA and PHY 3 Gbps NAND Cntrl. (BCH40)	1 Gb Ethernet + IEEE* 1588	
		Imaging Processing Unit Resizing and Blending Image Enhancement Inversion/Rotation		NAND Cntrl. (BCH40)	
	Security           RNG         Security Ontri.           TrustZone         Secure RTC           Ciphers         eFuses	Display and Camera Interface           HDMI and PHY         24-bit RGB, LVDS (x2)           MIPI DSI         20-bit CSI           MIPI CSI2         20-bit CSI	USB2 OTG and PHY USB2 Host and PHY	LP-DDR2, DDR3/ LV-DDR3 x32/64, 533 MHz	
	https://www.nxp.com/ processors/i-mx-6-proc cortex-a9-core:i.MX60	products/processors-and-microco cessors/i-mx-6quad-processors-h Q	ontrollers/arr igh-perform	n-processor ance-3d-gra	s/i-mx-applications- phics-hd-video-arm-
[14c.] a slave serial interface for coupling to a master serial interface through a clock signal line	In each of the Accused coupling to a master se output terminal.	l '474 i.MX Processors, the micro erial interface through a clock sig	oprocessor h nal line outp	as a slave so out terminal	erial interface for and a data signal line
output terminal and a data signal line output terminal	For example, each of the coupling to a master set processor) through a cl	he Accused '474 i.MX Processor erial interface ( <i>e.g.</i> , the I2C interf lock signal line output terminal ( <i>e</i>	rs has a slave face on the n e.g., SCL) ar	e serial inter naster/MCU nd a data sig	face (e.g., I2C) for and/or the host mal line output terminal

'474 Patent Claim	Representative NXP Product(s)
	( <i>e.g.</i> , SDA)).
	Chapter 35
	12C Controller (12C)
	35.1 Overview
	This chapter describes block-level operation and programming of I2C. The chapter is intended for a block-driver software developer. To understand how the block is integrated at the SoC level, a system software developer should see discussions of the block in the appropriate SoC-level chapter(s).
	References: This document assumes an understanding of the following document:
	The I2C Bus Specification, Version 2.1, by Philips Semiconductor
	The Inter IC (I2C) provides functionality of a standard I2C slave and master. The I2C is designed to be compatible with the standard NXP I2C bus protocol.
	NOTE
	Three independent I2C channels are available.
	I2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I2C standard allows additional devices to be connected to the bus for expansion and system development. See the connection diagram in the figure below.
	i.MX 6Dual/6Ouad Applications Processor Reference Manual, Document Number: IMX6DORM (Rev
	2, 06/2014) at 1893.



'474 Patent Claim	Representative NXP Product(s)						
	<b>35.4.1 I2C system configuration</b> After a reset, the I2C defaults to Slave Receive operations. Thus, when not operating as a master or responding to a slave transmit address, the I2C defaults to the Slave Receive state.						
	i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: IM 2, 06/2014) at 1897.	1X6DQRM (Rev					
	<b>NOTE</b> The I2C is designed to be compatible with the Philips <sup>TM</sup> I2C bus protocol. For information on system configuration, protocol, and restrictions, see the <i>I2C Bus Specification</i> , version 2.1, by Philips Semiconductors. The I2C supports Standard and Fast modes only.						
	i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: IM 2, 06/2014) at 1898.	1X6DQRM (Rev					

'474 Patent Claim					Represe	entative	NXP Pro	oduct(s)				
	35.7.3 I The I2C_I2 govern ope	2C Co CR is us ration as	ntrol Re sed to enal a slave or	egister ( ble the I2C a master.	I2Cx_I2	<b>CR)</b> 2C interru	pt. It also	contains b	its that			
	Address. base a	15	14	13	12	11	10	9	8			
	Read					D						
	Write											
	Reset	0	0	0	0	0	0	0	0			
	Bit	7	6	5	4	3	2	1	0			
	Read	IEN	IIEN	MSTA	MTX	ТХАК	0	(	)			
	Write	0	0	0	0	0	RSTA	0	0			
	Reset	U	U	U	U	U	U	0	0			
	i.MX 6Dual 2, 06/2014) 35.7.4 The I2C_	6Quad at 1913 <b>12C S</b> 12SR co	Applica tatus F	egister	• (I2Cx_ icate tran	Reference [12SR] saction di	irection ar	al, Docu	ment Nu		1X6DQR	M (Rev
	i.MX 6Dual 2, 06/2014)	/6Quad at 1914	Applica	tions Pro	ocessor	Referen	ce Manu	al, Docu	ment Nu	imber: IN	/IX6DQR	M (Rev

'474 Patent Claim	Representative NXP Product(s)								
	35.7.5 I2C Data I/O Register (I2Cx_I2DR)								
	In Master Receive mode, reading the data register allows a read to occur and initiates the next byte to be received. In Slave mode, the same function is available after it is addressed.								
	i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: IMX6DQRM (Rev 2, 06/2014) at 1916.								
	Address: Base address + 10h offset								
	Read 0 DATA								
	Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0								
	I2Cx_I2DR field descriptions								
	Field Description								
	15-8 This read-only field is reserved and always has the value 0. Reserved								
	DATA Data Byte. Holds the last data byte received or the next data byte to be transferred. Software writes the next data byte to be transmitted or reads the data byte received.								
	NOTE: The core-written value in I2C_I2DR cannot be read back by the core. Only data written by the I2C bus side can be read.								
	i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: IMX6DQRM (Rev 2, 06/2014) at 1916.								
[14d.] wherein the slave serial interface is	In each of the Accused '474 i.MX Processors, the slave serial interface is responsive to a read temperature command issued by the master serial interface to return to the master serial interface a								
responsive to a read temperature command	temperature value associated with the microprocessor.								
issued by the master serial interface to return to the master serial interface a temperature value	For example, in each of the Accused '474 i.MX Processors, the slave serial interface ( <i>e.g.</i> , I2C identified above) is responsive to a read temperature command ( <i>e.g.</i> , the read tempearture command requesting the result derived from the temperature monitor "TEMPMON" measurement) issued by the								

'474 Patent Claim		Representative NXP Product(s)	
associated with the microprocessor.	master serial above) to ret temperature	al interface ( <i>e.g.</i> , the I2C interface on the master/MCU and/or the host processor identies turn to the master serial interface a temperature value ( <i>e.g.</i> , the result derived from the monitor "TEMPMON" measurement) associated with the microprocessor identified a	fied ; above.
	35.7.5	I2C Data I/O Register (I2Cx_I2DR)	
	In Master next byte t addressed.	r Receive mode, reading the data register allows a read to occur and initiates the to be received. In Slave mode, the same function is available after it is d.	
	i.MX 6Dual/ 2, 06/2014) a Address: Base add Bit 15 1	l/6Quad Applications Processor Reference Manual, Document Number: IMX6DQRM at 1916. ddress + 10h offset	(Rev
	Read Write	0 DATA	
	Reset 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
	Field	Description	
	15–8 Reserved	This read-only field is reserved and always has the value 0.	
	DATA	Data Byte. Holds the last data byte received or the next data byte to be transferred. Software writes the next data byte to be transmitted or reads the data byte received.         NOTE:       The core-written value in I2C_I2DR cannot be read back by the core. Only data written by the I2C bus side can be read.	
	i.MX 6Dual/ 2, 06/2014) a	1/6Quad Applications Processor Reference Manual, Document Number: IMX6DQRM at 1916.	(Rev

'474 Patent Claim	Representative NXP Product(s)
	10.4.2.2 Thermal-aware power management
	The temperature sensor block (TEMPMON) implements a temperature sensor/conversion function. The block features an alarm function that can raise an interrupt signal if the temperature is above a specified threshold.
	Software may implement temperature aware DVFS for the ARM domain and the GPU domain, as well as temperature aware frequency scaling for other system components to ensure that both the frequency and voltage is lowered when the die temperature is above the specified limit.
	Software may also implement temperature aware task scheduling to ensure that non- critical tasks are suspended when the die temperature is above the specified limit.
	See Temperature Monitor (TEMPMON) for further details on temperature monitor functions and programmability options.
	Chapter 62 Temperature Monitor (TEMPMON)
	62.1 Overview
	based on a temperature-dependent voltage to time conversion.
	The module features an alarm function that can raise an interrupt signal if the temperature is above a specified threshold. A self-repeating mode can also be programmed which executes a temperature sensing operation based on a programmed delay.
	Software can use this module to monitor the on-die temperature and take appropriate actions such as throttling back the core frequency when a temperature interrupt is set.
	The high-level implementation of the temperature sensor is shown in the figure below.
	i.MX 6Dual/6Quad Applications Processor Reference Manual, Document Number: IMX6DQRM (Rev



'474 Patent Claim	Representative NXP Product(s)				
		TEMPMON_TEMPSENSE0n field descriptions			
	Field	Description			
	31-20 ALARM_VALUE	This bit field contains the temperature count (raw sensor output) that will generate an alarm interrupt.			
	19-8 TEMP_CNT	This bit field contains the last measured temperature count.			
	7	This field is reserved. Reserved.			
	6	This field is reserved. Reserved.			
	5-3	This field is reserved. Reserved			
	2 FINISHED	Indicates that the latest temp is valid. This bit should be cleared by the sensor after the start of each measurement.			
		INVALID — Last measurement is not ready yet.     VALID — Last measurement is valid.			
	1 MEASURE_	Starts the measurement process. If the measurement frequency is zero in the TEMPSENSE1 register, this results in a single conversion.			
	i.MX 6Dual/6Q 2, 06/2014) at 5	uad Applications Processor Reference Manual, Document Number: IMX6DQRM (Rev 163.			
	The Accused '4 temperature cor	74 i.MX Processors reads and returns the "TEMPMON" value in response to a read nmand issued by an external I2C master.			
	See, e.g.:				

'474 Patent Claim	Representative NXP Product(s)	
	<pre>if (status &amp; I2SR_SRW) { /* Master wants to read from us*/ dev_dbg(&amp;i2c_imx-&gt;adapter.dev, "read requested"); i2c_slave_event(i2c_imx-&gt;slave, I2C_SLAVE_READ_REQUESTED, &amp;value); /* Slave transmit */ ctl  = I2CR_MTX; imx_i2c_write_reg(ctl, i2c_imx, IMX_I2C_I2CR); /* Send data */ imx_i2c_write_reg(value, i2c_imx, IMX_I2C_I2DR); } else { /* Master wants to write to us */ dev_dbg(&amp;i2c_imx-&gt;adapter.dev, "write requested"); i2c_slave_event(i2c_imx-&gt;slave, I2C_SLAVE_WRITE_REQUESTED, &amp;value); https://patchwork.kernel.org/project/linux-arm-kernel/patch/20191009101802.19309-1- biwen.li@nxp.com/</pre>	